EDN®

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

AUGUST 17, 1995

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Industrial Electronics Special Issue

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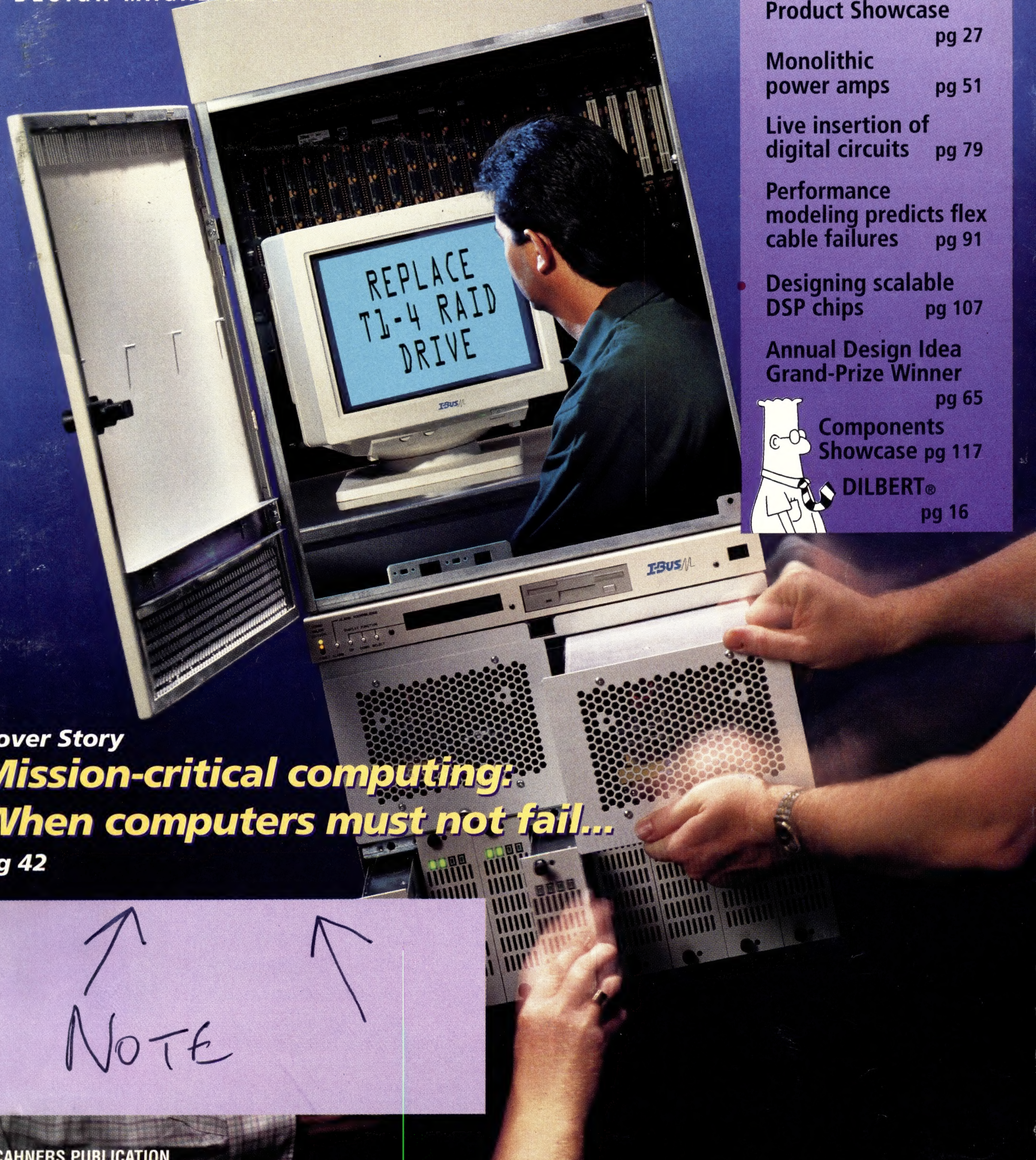

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Mission-critical computing: When computers must not fail...

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NOTE

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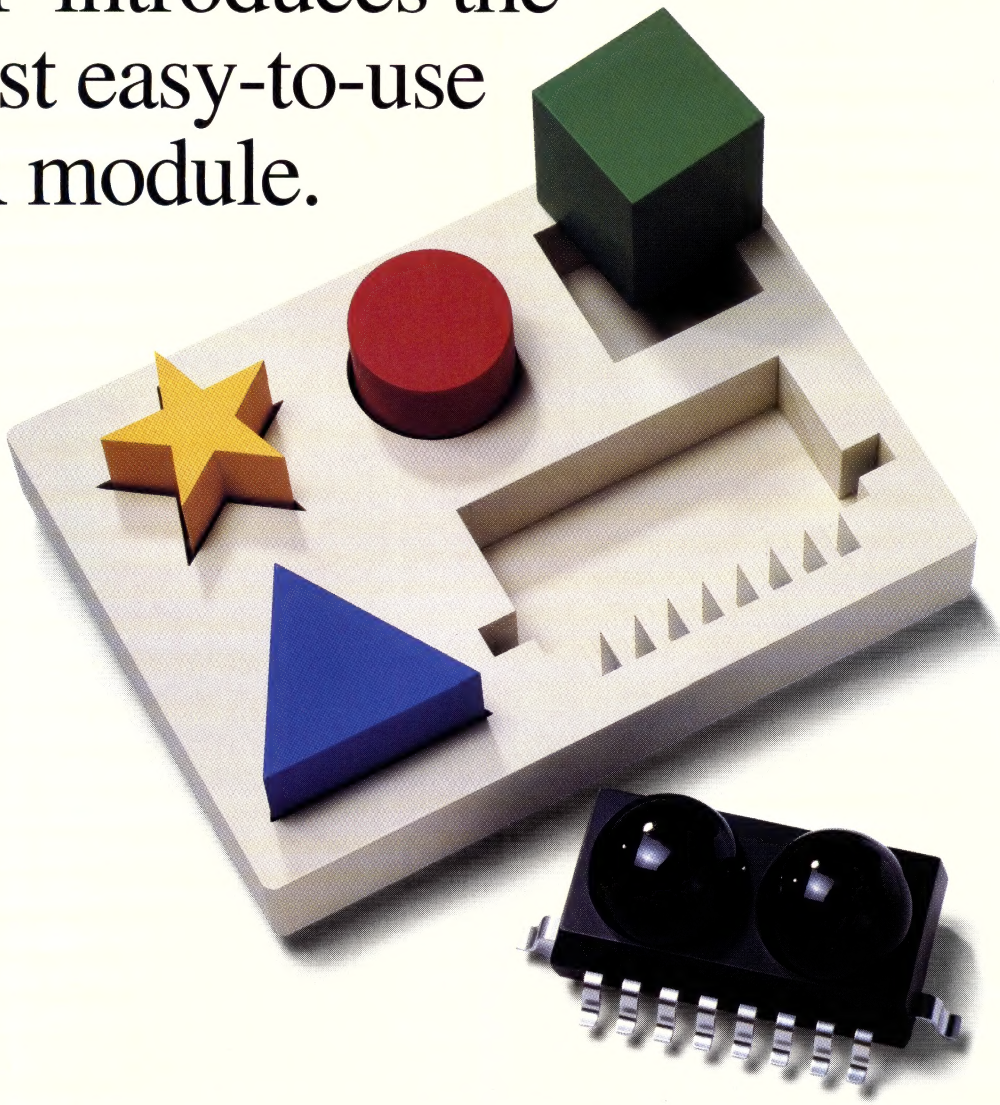

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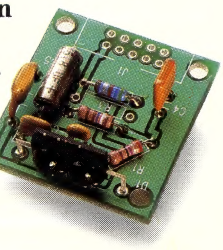

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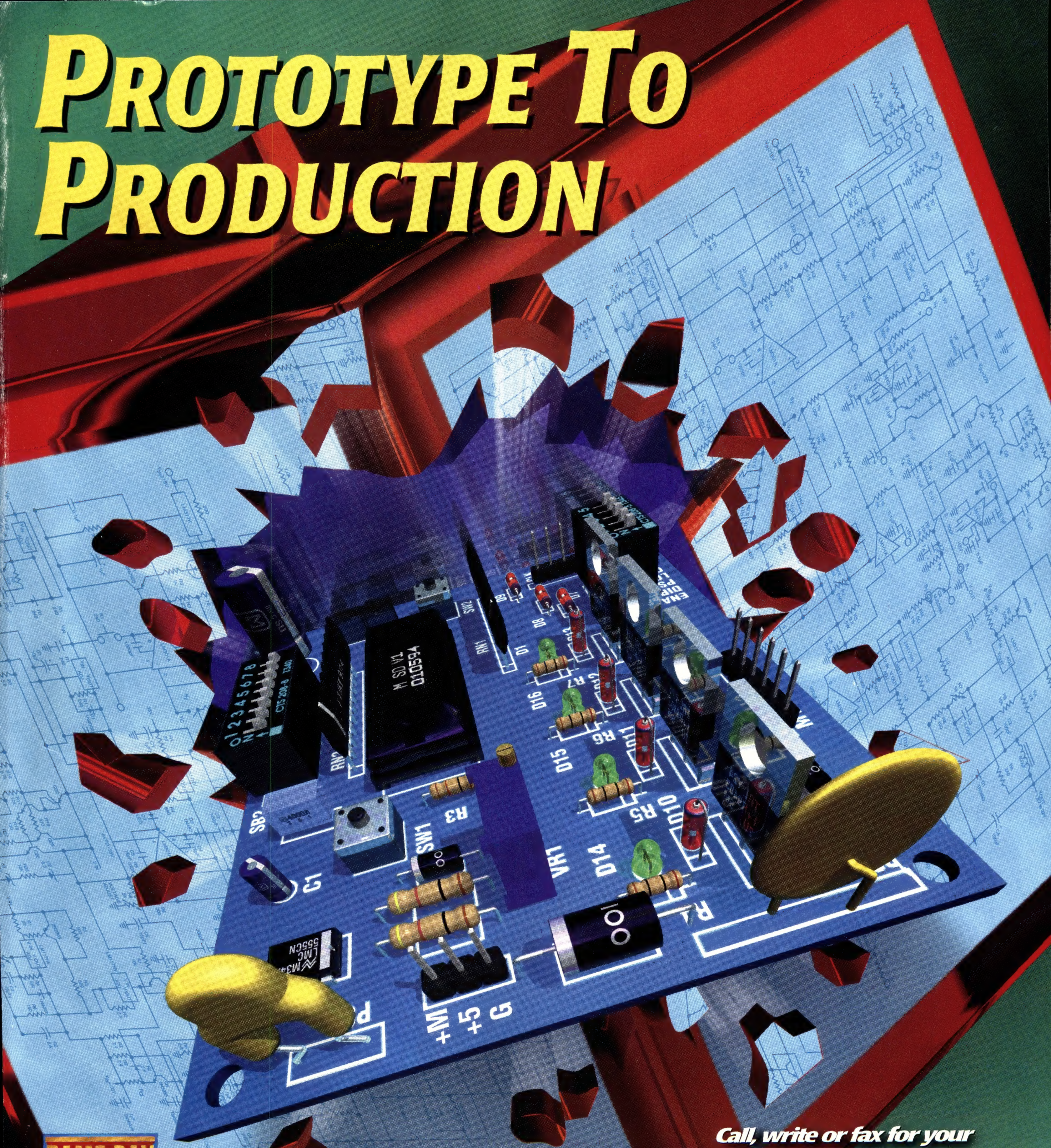

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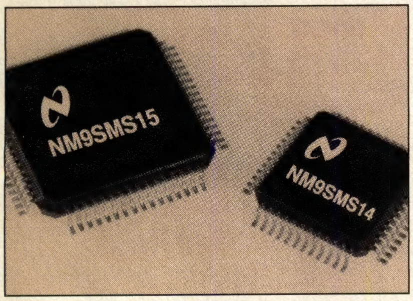

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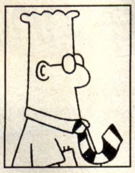

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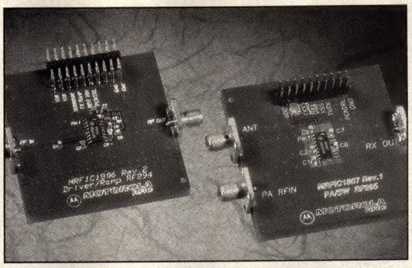

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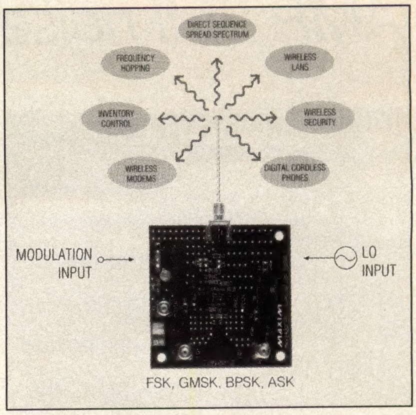

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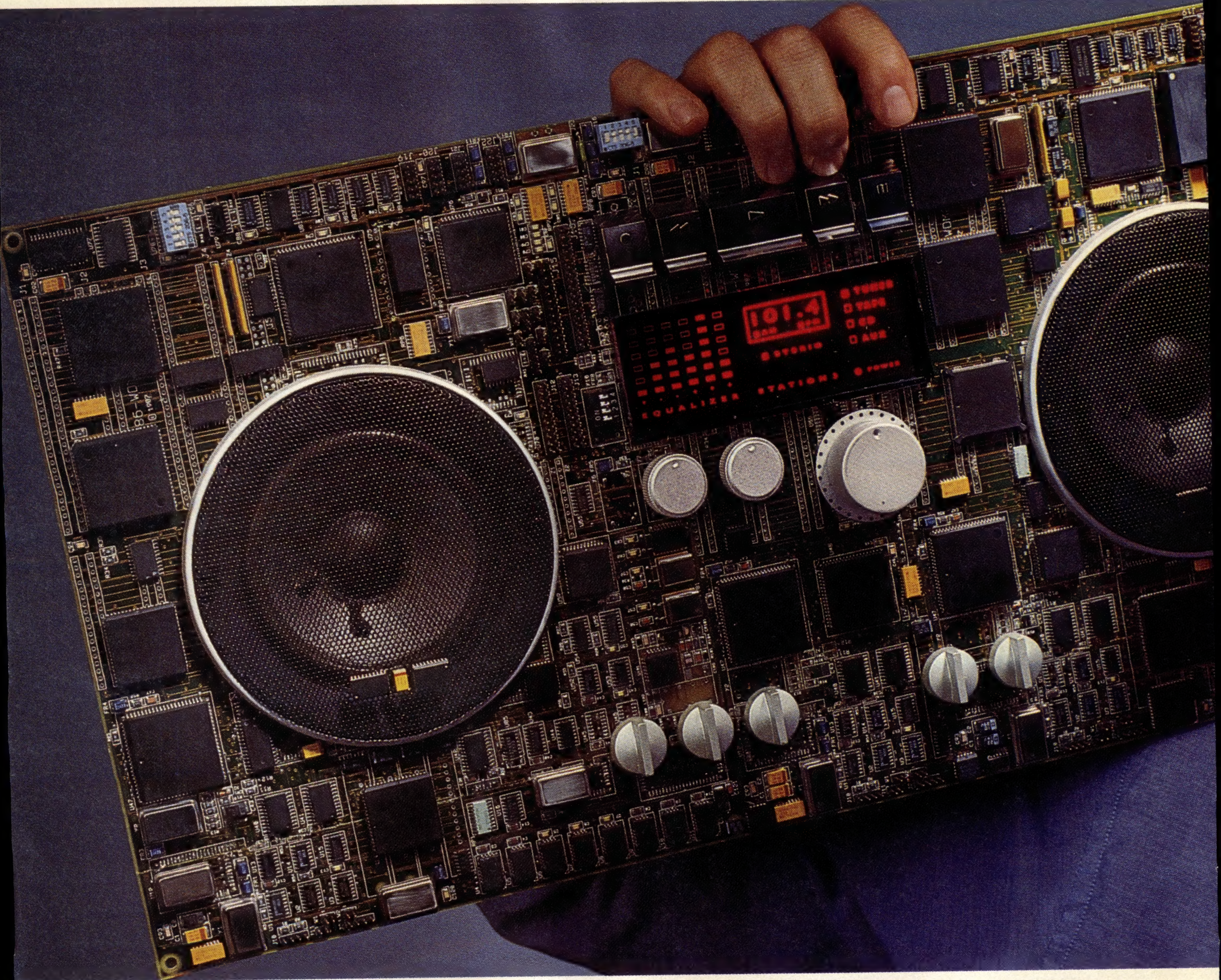
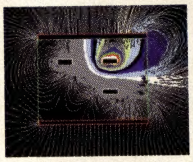
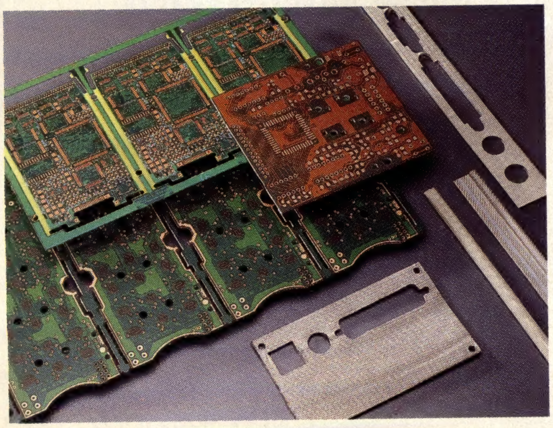




AMP Design, Simulation and Analysis Services prevent EMI problems even before the commitment to build.



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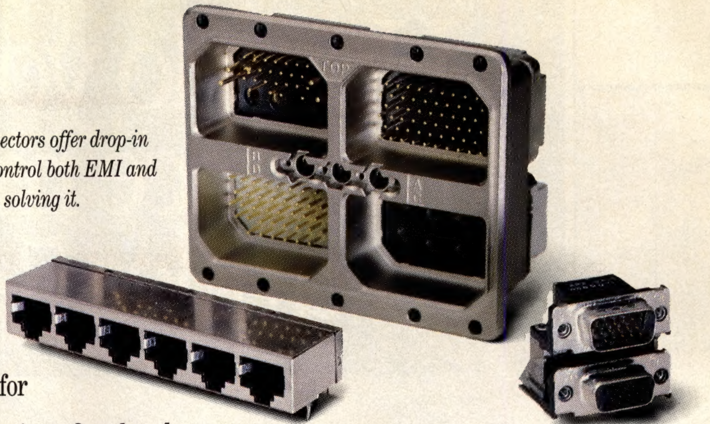
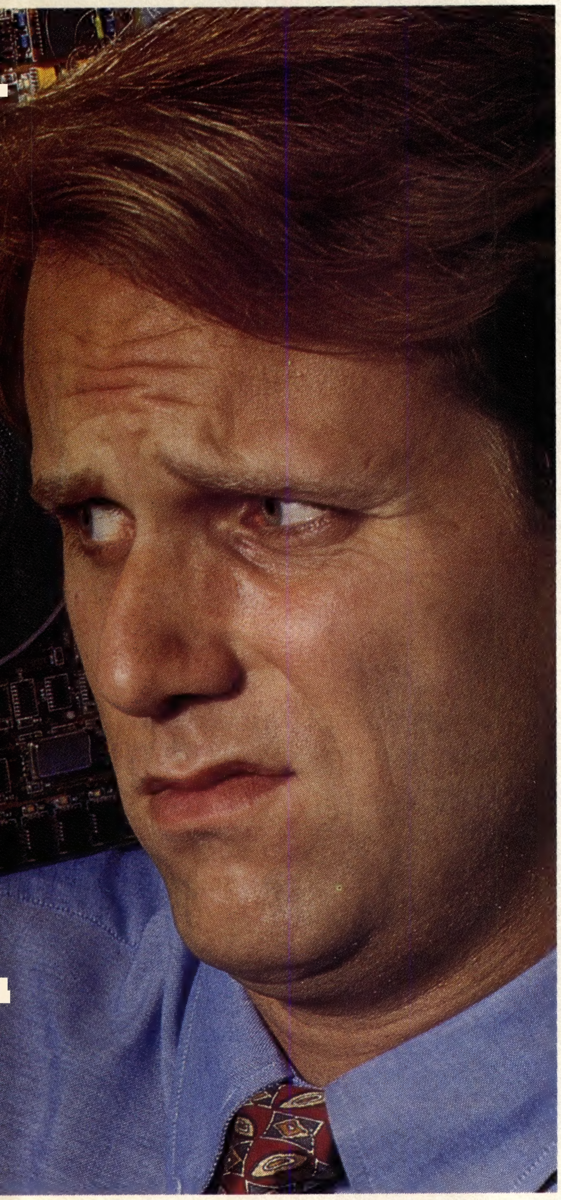


QuietLine filtered connectors offer drop-in footprint solutions to control both EMI and the cost associated with solving it.



Come to AMP for quiet solutions. Our decades of advancing interconnections and signal conditioning technology give us a uniquely effective perspective on EMI and its reduction.

Since the best time to control noise is before it starts, we've developed a simulation capability that helps eliminate EMI problems at your earliest design stage, prior to board fabrication.

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When it comes to filtered connectors, the industry's widest performance range – from ferrite through distributed element – and most respected core product technology are at AMP. Our QuietLine drop-in, replacement filtered connectors and shielded cable assemblies can be found almost anywhere there's an EMI- sensitive application.

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AMP, QuietBoard, QuietLine and QuietShield are trademarks.

For more information, call our Product Information Center at 1-800-522-6752 (fax 717-986-7575). AMP, Harrisburg, PA 17105-3608. In Canada, call 905-470-4425.

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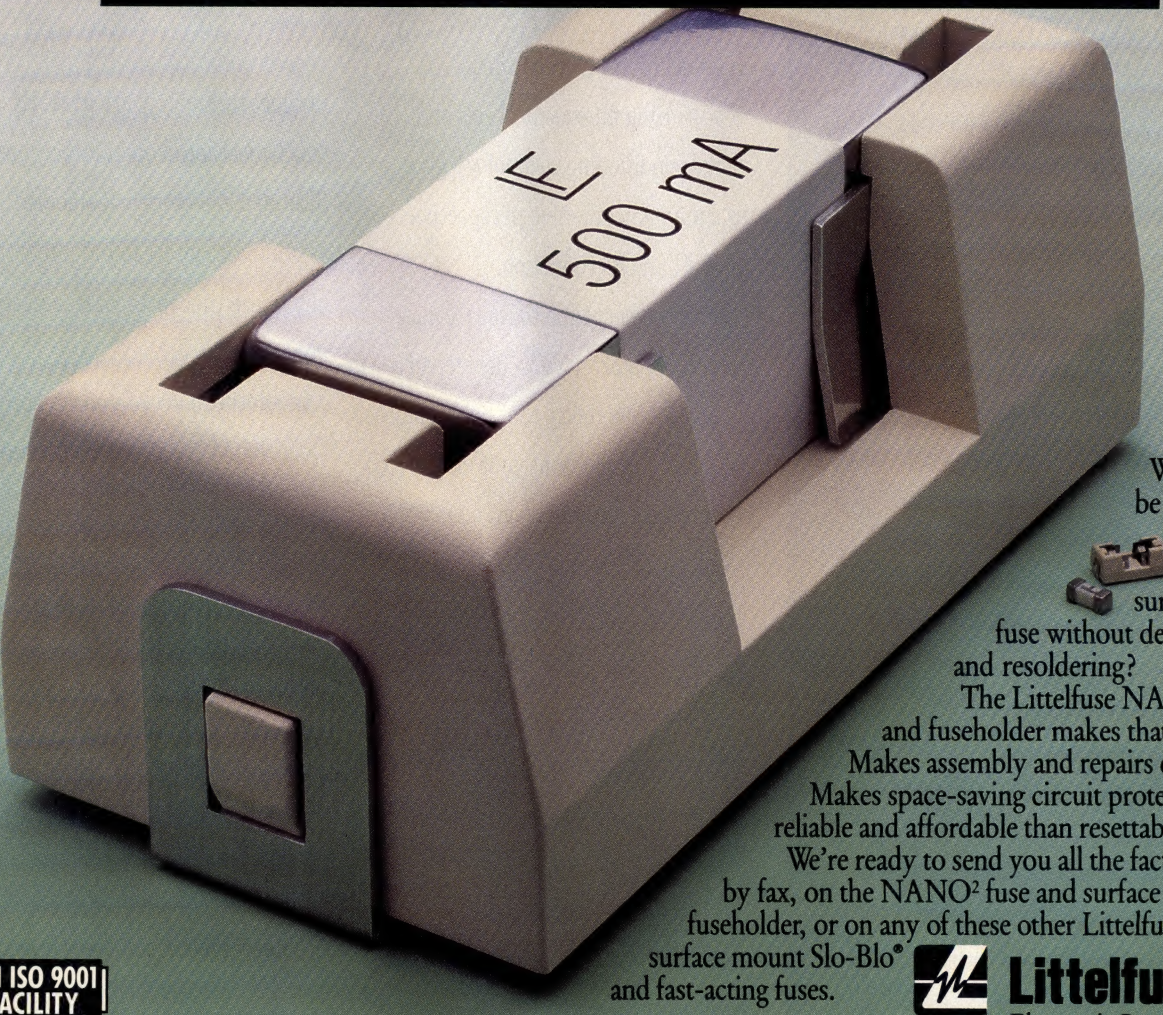

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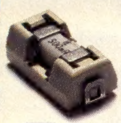				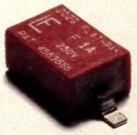
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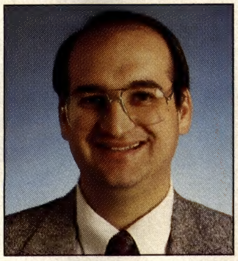
Calling all crooks



This is my year for telephone fraud. I've already had a brush with a fraudulent 900-number service being charged to my home phone (*EDN*, May 25, 1995, pg 9). Now, someone has stolen my business telephone credit-card number. A call from Sprint was waiting on my answering machine when I arrived at work on a recent Monday morning. Because of an unusually high number of telephone calls from California to Mexico charged to my credit-card number, Sprint correctly concluded that my number had been compromised and terminated the credit card.

My first action was to check for my credit card. It was right where it was supposed to be. Of course, I don't generally carry the actual plastic credit card. Most public phones won't accept the plastic card so, long ago, I memorized the 14-digit number and now just punch in the number when placing a call. I'm also aware that there are numerous credit-card thieves out there, so I punch in the number fairly rapidly and try to cover the keypad, as I've read you should.

Now, when personally confronted with the problem, I thought back over the previous week's events to determine how someone might have stolen my credit-card number. It shouldn't have been hard, as it turns out. The week before my credit card decided to take a Mexican vacation, I attended the Design Automation Conference in San Francisco. I made many long-distance calls at pay phones. Many of these pay phones have easy-to-read displays that, among other things, display the numbers you punch in.

My credit-card number appeared, billboard style, every time I made a call on one of these phones! It sort of brings to mind the giant MCI billboards showing how much people save by using the company's service. Instead of giant dollar amounts up in lights on the billboard, substitute my credit-card number.

My credit-card number appeared, billboard style, every time I made a call!

Our information society is now in full swing, and a lot of information is better left private. I'm convinced someone was able to rip off my number through the poor design of these public pay phones. If you are working on any sort of public information system, make sure all aspects of information security are at the top of your design agenda.

Steven H. Leibson

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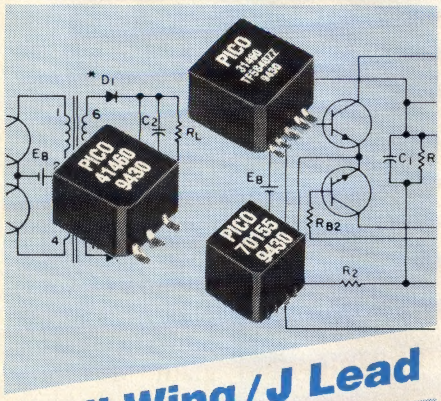

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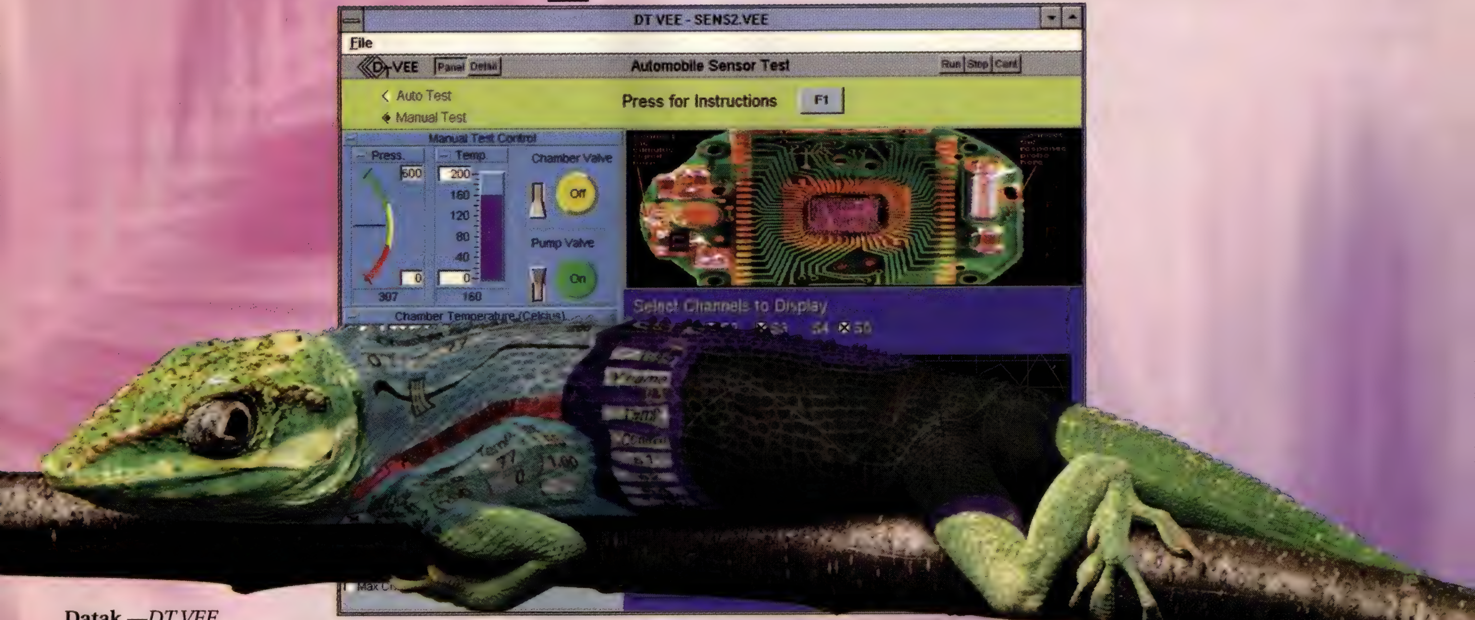

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CIRCLE NO. 97

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CIRCLE NO. 98

OUT IN FRONT

WHAT'S HOT IN THE DESIGN COMMUNITY

EDITED BY FRAN GRANVILLE

Multichannel sigma-delta A/D converter overcomes limitations

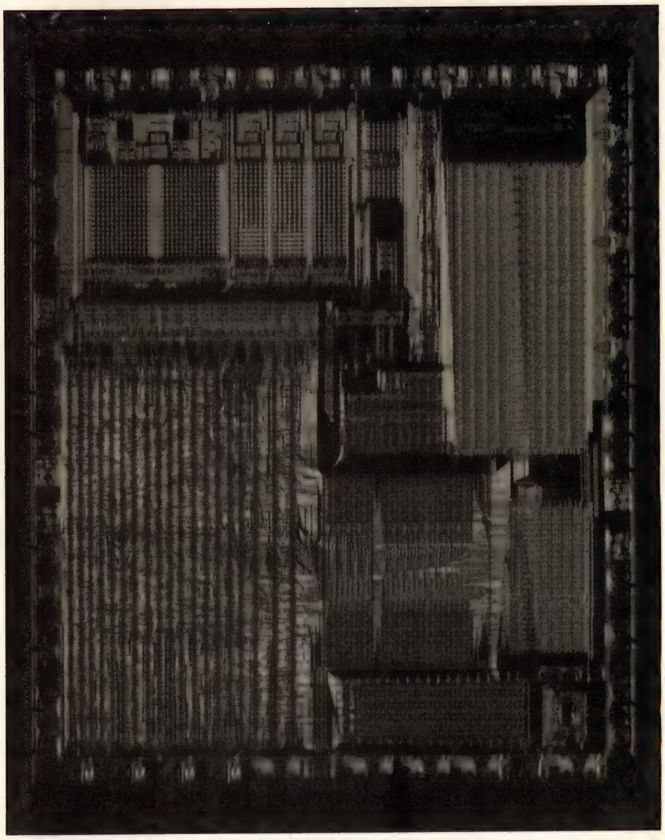
Handling eight analog input channels and incorporating an on-chip multiplexer and microsequencer, Harris Corp's HI7188 programmable measurement system provides 16-bit resolution at 240 samples/sec per channel. Using a proprietary channel-management technique, the subsystem avoids the traditional shortcomings of multiplexed, multichannel sigma-delta converters, including the dead time or loss of samples when scanning from channel to channel. This latency results from the converter's digital-filter pipeline reinitializing its data stream.

The IC suits sensor-based applications, such as temperature, pressure, and weight, in process control and instrumentation for input ranges of 20 mV to ±2.5V. You can reconfigure the IC on the fly by downloading a word for each channel without data loss or lag time. A user-set control word determines input sequencing, including repeats; channel gain of one to eight; and normal vs calibration mode. The microsequencer manages overall operation and details.

Power dissipation from a ±5V supply is 40 mW, and the converter provides –120 dB of digital filtering of 50/60-Hz line noise. Integral nonlinearity is 0.0015%. The HI7188 is available in a 40-lead plastic DIP and 44-lead QFP package. Price is $39.95 (100).—by Bill Schweber

Harris Semiconductor Corp, Melbourne, FL. (800) 442-7747, ext 7348.

Circle No. 400



The HI7188 eight-channel, 16-bit A/D converter features an internal microsequencer that manages all channel functions; the proprietary IC architecture avoids historical sigma-delta converter latency problems.

Switch-level option added to Verilog simulation

RCsim from interHDL, a switch-level simulation option for the Viper Verilog HDL simulator, addresses a historical problem of behavioral and register-transfer-level (RTL) simulators: their inability to spot gate- and device-level timing problems. By simulating detailed circuit behavior in complex ICs, RCsim helps you spot hidden timing problems due to phenomena such as charge sharing and race conditions.

RCsim dynamically calculates a steady-state solution along with transitional delays for every switch node in a circuit. The switch-level simulation algorithms of RCsim integrate with Viper's behavioral and RTL simulation algorithms. The company claims that RCsim's simulation accuracy is within 5% of Spice with a simulation speed at least two orders of magnitude faster than Spice. RCsim operates on process and device characteristics. It has a utility program that runs Spice and generates a technology file from process and transistor parameters from a silicon foundry. After the one-time generation of the technology file, RCsim uses the file as a basis for timing analysis of a chip or portions of a chip.

RCsim provides a way, within an HDL simulation environment, to analyze potential timing problems in critical portions of a chip. If you locate a problem, you can change

(continued on pg 16)

the configuration of the cell containing the problem or use a functionally equivalent cell from the library with different driving or delay characteristics, which often means one with different-sized transistors driving the output of the cell. You generally would not perform this level of analysis over an entire chip. You would use it in critical cells where device-related timing problems are likely to occur, however.

The RCsim option to interHDL's Viper simulators is available for Windows, Windows NT, and Unix. RCsim costs $4000 for the PC version and $10,000 for the Unix version. The Viper simulator costs $5000 for PCs and $12,500 for Unix systems.—by Jim Lipman

interHDL, Los Altos, CA. (415) 428-4200.

Circle No. 401

Plug and Play capability for add-in cards fits on a chip

The NMS95MS14 and NM95MS15 memory-enabled devices from National Semiconductor provides Plug and Play (PnP) capability for ISA bus systems. The devices allow add-in-card manufacturers to offer products that take advantage of Windows 95 PnP functions. The chips integrate a state machine, switching logic, an address decoder, and an EEPROM onto one chip.

For adapter functions that require additional nonvolatile memory to store card-specific information, such as the communication parameter and Ethernet address, the chip can access 4 kbits of extra EEPROM through a Microwire interface.

The NM95MS14 connects directly to the ISA bus, supports one logical device, and provides DMA and extended-interrupt operating modes. The NM95MS15 implements the PnP specification; connects directly to the ISA bus; and supports two logical devices, as many as four I/O-chip selects, two memory-chip selects, and 20 address lines. The chip operates in DMA, extended-interrupt, and extended-DMA modes. The primary benefit of having three modes is that a card manufacturer can mix and match any adapter's requirements with one chip rather than having an inventory of larger packaged chips or multiple chips.

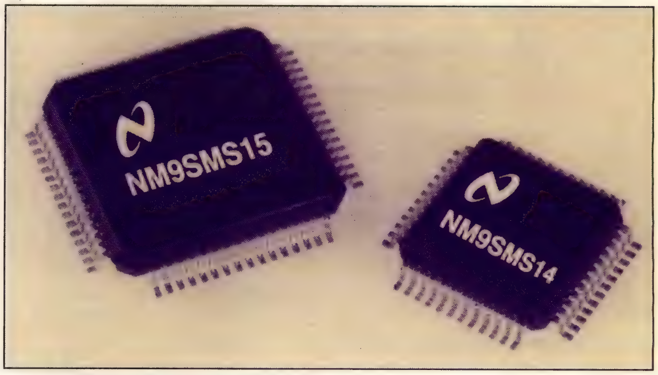
Both devices feature an integrated EEPROM. The NM95MS14 offers 2 kbits for PnP resource allocation and 4 kbits for external Microwire access. The NM95MS15 offers 4 kbits for PnP resource allocation and 4 kbits for external Microwire access.

The NM95MS14 comes in a 48-pin TQFP and should be in production in the third quarter. The NM95MS15 comes in a 64-pin TQFP and should be in volume production by year-end. The company is shipping samples and limited quantities to beta sites and selected potential customers. Both chips will sell for less than $4.

—by John Gallant

National Semiconductor, Santa Clara, CA. (408) 721-8387.

Circle No. 402



National's NM95MS15 and NM95MS14 contain the functions to implement the Plug and Play capabilities of Windows 95 on a single chip.

DILBERT® by Scott Adams
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CIRCLE NO. 69

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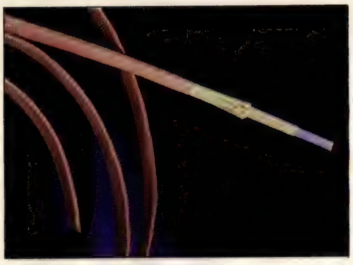

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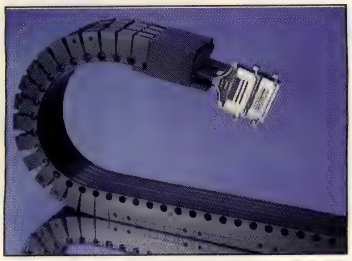

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Gore offers a quiet, cost effective alternative to existing rolling flex cable tracks. Our lightweight, modular PROFILE track system offers smoother, faster acceleration with fewer moving parts to create dust. Its open structure also allows easy installation and replacement of cables.

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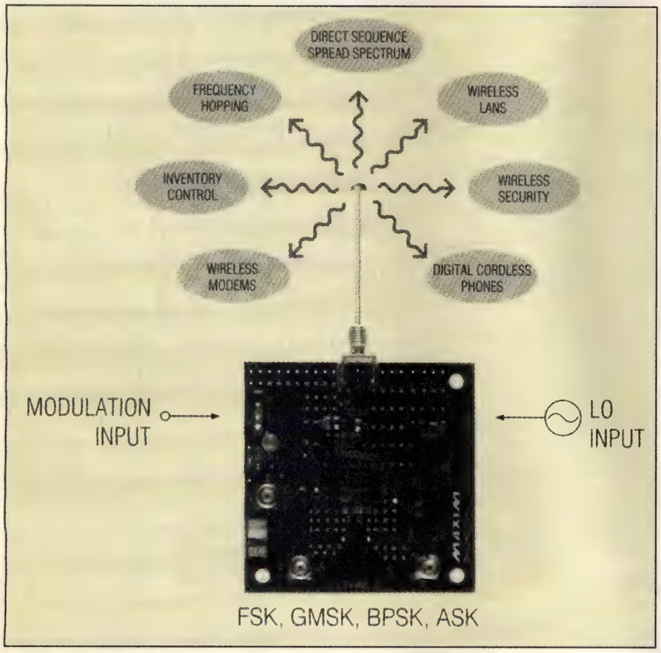
CIRCLE NO. 74

PROLIFERATION OF RF FUNCTIONAL-BLOCK ICs EASES DESIGN CHALLENGE

Vendors are putting the key functional blocks and subsystems for RF transmitters and receivers into compact ICs, reducing size and the need for discrete components and circuitry. For the 800- to 1000-MHz band, including the 902- to 928-MHz industrial, scientific, and medical band, Maxim's MAX2402 transmitter integrates a double-balanced mixer, a buffered, local-oscillator input port, a variable-gain stage, and a power amplifier into a 20-pin SSOP device. In a typical application, a digital baseband signal mixes with the local oscillator signal, producing a binary phase-shift-keyed modulated signal at the antenna. Output power is at least 100 mW into a 50Ω load, from a single 5V supply.

Inputs are not restricted to digital signals: The baseband modulation input is linear over a 3V range, so the device can form an AM or FM analog transmitter. The internal variable-gain amplifier has 40 dB of adjustment range, and the output power amplifier (20-dBm power) has a bias adjustment to improve efficiency and minimize distortion; local oscillator range is –6 to +6 dBm. In shutdown mode, the IC switches to draw under 1 μA in less than 10 μsec. The IC costs $3.59 (1000).

Maxim Integrated Products, Sunnyvale, CA. (408) 737-7600, ext 6087. **Circle No. 403**

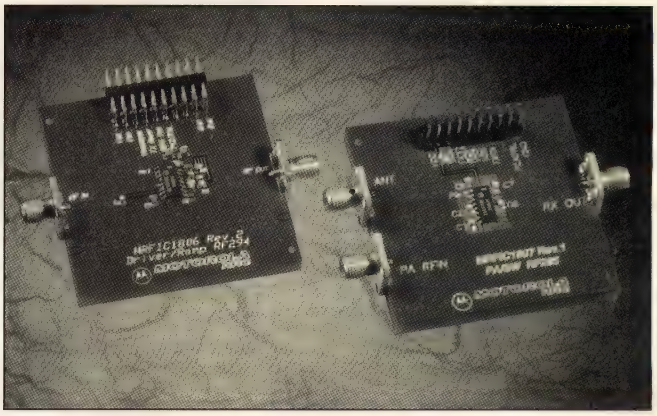


Maxim's MAX2402 transmitter integrates a double-balanced mixer, a buffered, local-oscillator input port, a variable-gain stage, and a power amplifier into a 20-pin SSOP device.

Motorola provides transmit- and receive-function ICs for the 1500- to 2200-MHz band, including 1.9-GHz personal communication systems, such as Digital European Cordless Telephone (DECT) and Japan's Personal Handy System (JPHS). The GaAs MRFIC1806 comprises a driver amplifier and ramp circuit to control attack and decay times and to minimize adjacent-channel interference. The devices come in 16-pin SOICs and use supplies ranging from 3 to 5V. The ICs produce a 21-dBm output from a 0-dBm input.

The MRFIC1806 drives the companion MRFIC1807 power amplifier and transmit/receive switch, which also comes in a 16-pin SOIC. This GaAs IC produces up to 27-dBm output into a 50Ω load from a 19-dBm input. A CMOS logic-level signal controls the switch and can handle up to 28 dBm through the transmit path; switch receive-path insertion loss is less than 1 dB. In small quantities, the MRFIC1806 costs $7.30, and the MRFIC1807 costs $10.50.—by Bill Schweber

Motorola Inc, Phoenix, AZ. (602) 244-6108.
Circle No. 404



Motorola's 1.9-GHz GaAs ICs provide transmit and receive functions for the 1500- to 2200-MHz band, including personal communications systems.

Broad-based technical-information access comes to the desktop

Information Handling Services (IHS) has launched Congruity, a technical-information and component-selection system. The client-server-based product gives you desktop search capabilities and access to internal and external component data and supporting documentation, such as industry standards and military specifications. Congruity comprises a client-server architecture for searching and retrieving information, databases containing the underlying data, component-management and

(continued on pg 22)

TMS320C80
DSP

Now you can fly first-class at coach pricing.

The TMS320C80: the industry's highest performance DSP is now priced to move even faster.

The 'C80 from Texas Instruments, which breaks all industry performance records, is now breaking new records for affordability. With volume production reducing device costs by 55% and 80% lower tool costs, the 'C80 gives you first-class performance at affordable prices. Its high level of single-chip integration gives you the power and flexibility to perform your most demanding audio, video, image processing and telecommunications applications.

TI's comprehensive set of TMS320 DSP tools also supports the 'C80. Our new PC tools can even bring this development environment to your own PC. If you'd like more information on the 'C80 and how you can get an additional 20% discount off our PC or Sun™ tools, please call **1-800-477-8924, ext. 4002.** *Then let the 'C80 take your designs to new heights.*

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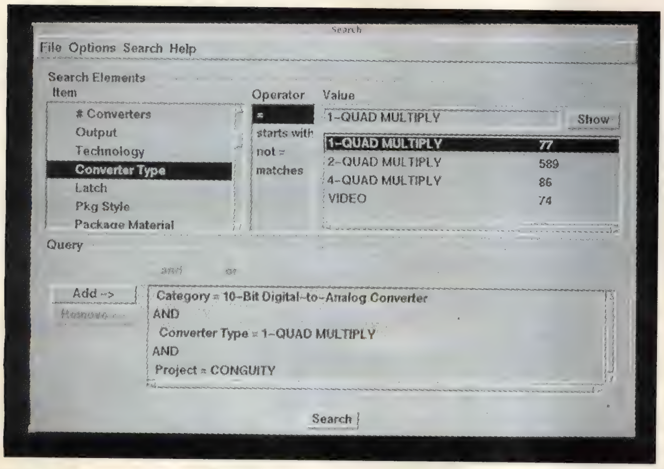
08-1194

system-administration utilities, and interfaces to several CAE systems.

The client-server architecture supports Hewlett-Packard servers and HP, Sun, IBM RS 6000 and PC clients. The company plans to begin Macintosh client support this year. Congruity supports the native windowing system and interface—Motif on Unix, Windows on PCs, and Mac on the Macintosh—on each client platform. An application-programming interface lets you easily integrate Congruity with external CAE or internal systems.



1-QUAD MULTIPLY

1-QUAD MULTIPLY 77
2-QUAD MULTIPLY 589
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VIDEO 74

Category = 10-Bit Digital-to-Analog Converter
AND
Converter Type = 1-QUAD MULTIPLY
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With Congruity, you can search for components by part number, attribute values, and preferred parts lists.

IHS Xpert databases from more than 18,000 data sources and comprising more than 13 million pages of information supply internal data to Congruity. Available Xpert databases include those for semiconductors, military specifications and standards, industry standards, and vendor catalogs. IHS updates data every seven to 60 days and plans to add databases for passive components, military and commercial connectors, and plastic materials.

You can search the databases for components and documentation through a variety of search paths, including document or part numbers; keyword, including Boolean operators; class or category; and parametric values. You can also add internal component information to Congruity. Such information might include corporate part numbers, supplier cross-references, attributes describing corporate parts, preferred parts lists and links to externally managed information.

IHS is integrating Congruity with third-party CAE, data-management, and decision-support systems. Mentor Graphics, Cadence Design Systems, and Intergraph Electronics comprise the first group of partners working with IHS. Prices for Congruity start at $73,000, which includes a year's subscription to both the software and the Xpert databases for five concurrent users. Prices for Congruity Lite, a version with all of the features of Congruity except the ability to add data, start at $37,000.

Information Handling Services, Englewood, CO. (303) 790-0600
Circle No. 405

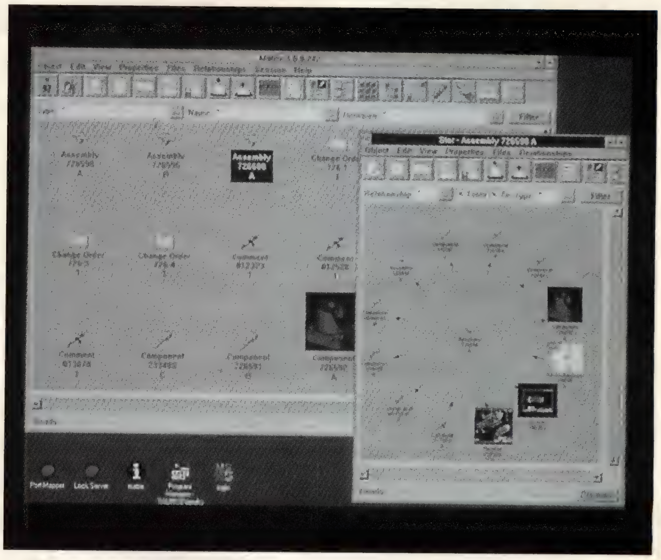
Also addressing the product-data-management market, Adra Systems has introduced the third version of its object-based Matrix System. Matrix integrates data management, work flow, and communications through a graphical user interface. Like Congruity, Matrix is a cross-platform, client-server product that supports a variety of PCs and Unix-based platforms. Matrix also supports many operating systems, including AIX, Digital Unix, HP-UX, Irix, Solaris, SunOS, Windows, Windows NT, and Windows 95.

Matrix lets you store graphical samples of drawings, layouts, reports, and other files for ease of interpretation when reviewing information. This feature relieves you of the burden of remembering unfamiliar naming conventions and codes. In Matrix, product structures can include both electronic and nonelectronic data. You can represent the interrelationship of assemblies, subassemblies, components, and discrete parts. You can also establish rules to automate the checking of relationship accuracy.

Matrix 3.0's new features include electronic-mail capability to other Matrix systems and the Internet, additional graphical information browsers, and drag-and-drop capability for linking information and defining relationships between objects. Prices for Matrix 3.0 start at $35,000 for an initial 20-user license. Additional user licenses cost around $1200 each.

—by Jim Lipman

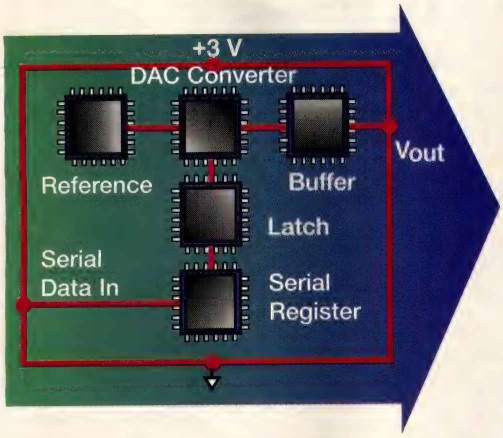
Adra Systems/Matrix Division, Shelton, CT. (203) 944-2020.
Circle No. 406



Matrix's Flat Browser (left) and Star Browser (right) illustrate the visual nature of the Adra system. The Star Browser displays the relationships of the several components related to one assembly.

The First One-Chip 3-V DAC For Today's Battery-Powered, Portable World.

The Old Multichip Way


+3 V
DAC Converter
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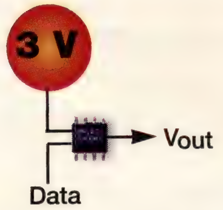
Buffer
Vout
Latch
Serial
Data In
Serial
Register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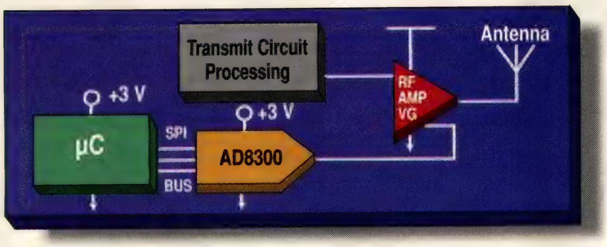
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Key performance features include high 12-bit resolution for precise level settling; ±1 LSB maximum DNL to assure monotonicity for adjustment applications; 0.5 mV/bit output span for easy programmability; 3.6 mW power consumption from +5.5 V down to 2.7 V to maximize battery life; and a three-wire serial interface to simplify SPI and other popular interfaces in a double buffered format.

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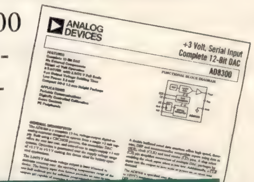
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CALL FOR PAPERS

DSP^x 1996—The Signal Processing Applications Conference & Exposition

March 11-14, 1996, San Jose Convention Center, San Jose, CA

ABSTRACTS DUE: SEPTEMBER 17, 1995

Take part in an evolution! DSP^x has matured into the most comprehensive electronics application design conference ever. DSP^x 1996 will feature hundreds of presentations on applications of **DSP, advanced analog, mixed signal, ASIC, microprocessors/microcontrollers, EDA, and test/measurement technologies**—all of the technologies used by the electronics design team. In addition, DSP^x 1996 will provide application solutions that meet the needs of the communications, computer, consumer, aerospace, military, medical, automotive, and industrial markets.

We are looking for papers from design engineers that work in any of the above markets, with original application solutions that involve any of the technologies listed below.

AUDIO/VOICE/SPEECH
- **Recognition/Synthesis**
- **Compression/Coding**
  - Simultaneous Voice & Data (SVD), Cellular/PCS, CELP, Secure Speech
- **Professional Audio**
  - Synthesizers, Mixers, Special Effects, Editing, DAT
- **PC Based**
  - Multimedia, Computer Telephony Integration (CTI), Voice Messaging, Modems, Speakphone, Fax/Data Modem
- **Consumer**
  - DCC, DBS, DAT, DAB, Mini-disc

VIDEO/IMAGING
- **Recognition**
  - OCR, Machine Vision, Target Identification, Handwriting Recognition, Radar/Sonar
- **Compression**
  - Full Motion, Still Frame, JPEG, MPEG1, MPEG2, MPEG4, Fractals, Wavelets
- **Videoconferencing**
  - H.320, H.324, Proprietary
- **Image Processing**
  - Medical Applications, Consumer Applications, Military/Aerospace
- **Applications**
  - Entertainment, Document Processing

CONTROLS
- **Noise/Vibration**
  - Noise Cancellation, Acoustic Echo Cancellation, Electronic Echo Cancellation
- **Motor Control**
  - Industrial, AC Induction, DC Brushless, 3-Phase AC, Variable Speed, Power Factor Reduction
- **Motion Control**
  - Robotics, Servo Mechanism, Industrial
- **Automotive**
  - Active Suspension, Anti-knock, ABS, Noise Cancellation

COMMUNICATIONS
- **Wired**
  - PSTN/Modems (V.32BIS, V.34), LAN, WAN, ADLS/HDSL/ISDN/ATM, Cable/Cablephone
- **Wireless**
  - Cellular (GSM, IS54, IS136, EDC, CDPD), PCS, Infrastructure, Satellite, RF
- **Global Positioning Systems (GPS)**
- **Simultaneous Voice & Data (SVD)**
- **Video Conferencing**
- **Computer Telephony Integration (CTI)**

INSTRUMENTATION
- **Medical/Diagnostics**
  - CT, MRI, ECG, EEG, EMG, Ultrasound, Nuclear Imaging, DNA Synthesis/Sequencer, Video Endoscopy, Patient Monitoring
- **Data Acquisition**
  - Sensors, Signal Conditioning
- **Signal Analysis**
  - Algorithms, Filtering, Spectral Analysis, Transforms
- **Test/Measurement**
  - Digital Oscilloscopes (DSO)
- **Virtual Instrumentation**
- **VXI**
- **Communications Testers**
- **LAN Testers**

CORE TECHNOLOGY
- **DSP**
  - Parallel Processing, NSP, Development Tools, Development Languages, Reconfigurable DSPs
- **ASIC**
  - DSP Core, Mixed-Signal ASICs, Function-Algorithm-Specific ICs (FASIC)
- **Microprocessor/Microcontroller**
- **Memory**
  - ROM, RAM, SRAM, DRAM, flash, RDRAM, ARAM, RAM BUS, SDRAM
- **Converters**
  - Analog to Digital (A/D), Digital to Analog (D/A), CODECs
- **Analog/Linear**
  - Signal Processing, Power, RF, Filters
- **EDA**
  - High-Level-Language Tools, System-Level Design, Chip Synthesis, Code Synthesis
- **Emerging Standards**
- **Power Management**
  - Hardware, Software

Please submit one or more abstracts of your paper by fax to Robert Williams, Director of Industry Development, at (203) 840-9345, or by e-mail at robertwi@ix.netcom.com. Using a font size no smaller than 10 pt, abstracts should be **no more than one page in length.**

1. Abstracts should include your name, title, company, address, phone, fax, and e-mail address.

2. Classify your paper by each of the following 3 categories: (Please **use all 3 categories** for your paper.)
- **Market Segment** (Communications, Computers, Consumer, Aerospace/Military, Medical, Automotive, Industrial)
- **Application Category** (Audio/Voice/Speech, Video/Imaging, Controls, Communications, Instrumentation, Core Technology), and the applicable **Sub-Category** (see above technology list)
- **Technology Category** (DSP, Analog, Mixed Signal, Microprocessor/Microcontroller, EDA, Test/Measurement).

3. Please specify what **Internet newsgroups/websites and publications** your paper would most be of interest to. The abstract must be non-commercial, applications-oriented solutions. **Papers which describe a company or its products rather than the technology application will not be accepted. Please Note: Due to the volume of responses, ONLY IF YOUR ABSTRACT IS SELECTED will you receive further information on the format and guidelines to be used for paper development/submission.**

Order Motorola 68HC705J1A development kit.

Create amazing design.

Enter design contest.

Win Ford Explorer.

Ride off into sunset.

Live happily ever after.

Put the pedal to the metal and enter Motorola's new 68HC705J1A design contest. You could be awarded a 1996 Ford Explorer†.

The contest begins May 15 and ends October 31, 1995. And entering is easier than you think.

First, order your 68HC705J1A development kit from your local distributor at the low introductory price of just $99*! It's packed with the hardware, software and documentation you need to get rolling.

Then, think of a great way to enhance your 8-bit design with this versatile new microcontroller from Motorola. The 68HC705J1A is the perfect One-Time-Programmable (OTP) device for applications ranging from wristwatches to satellites. Enter the contest with your design idea and we'll send you a free T-shirt.

Finally, sit back and think about winning. Four entrants will each win a family entertainment center. And the grand prize winner will drive away in a '96 Ford Explorer.

But think fast, because the contest comes to an end October 31! The complete development kit and entry form, contest rules and details are available only from your local Motorola distributor.

For more information on the 68HC705J1A, or for a list of distributors, call Motorola at 1-800-765-7795, ext. 814, fax us at 1-800-765-9753, or write P.O. Box 13206, Austin, Texas 78711-9855.

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† Ford Explorer shown is 1995 MY. Actual prize awarded will be a 1996 Eddie Bauer model with preferred equipment package. *Suggested price. Motorola and Ford Motor Company employees, contest judges and their families are not eligible. Contest valid for residents of North America only. Contest void where prohibited by law. See contest rules and entry form for details. Ⓜ and Motorola are registered trademarks of Motorola, Inc. ©1995 Motorola, Inc.

HOTTEST REAL-TIME DESIGN WIN

Microware's OS-9 for interactive television

Microware's OS-9 Real-Time Operating System is the acknowledged leader in real-time system software for industrial and intelligent consumer electronics applications. Now, OS-9 is firmly established in the exciting new industry of interactive television.

OS-9 — AN EMERGING STANDARD

OS-9 is becoming the standard in interactive television through its acceptance and use by:

- **Set-Top Box Manufacturers** — More than 20 major manufacturers are building OS-9-based set-top boxes.
- **Network Providers** — OS-9's flexibility handles all sizes of networks, ranging from small-scale "private" systems to telephone- or cable-based WANs.
- **Video Server Providers** — Both low-end and high-end server platforms can target OS-9.
- **Content Providers and Application Developers** — Can choose OS-9-based development software from Microware and allied third parties.

OS-9 FOR ANY PROJECT

While interactive television is its most visible design win, OS-9 also powers applications and environments ranging from robotics to medical instrumentation, traffic control and aerospace engineering. OS-9's high-performance modular architecture, broad I/O support, tightly integrated development environment and unsurpassed technical support make it the obvious choice for your next development project.

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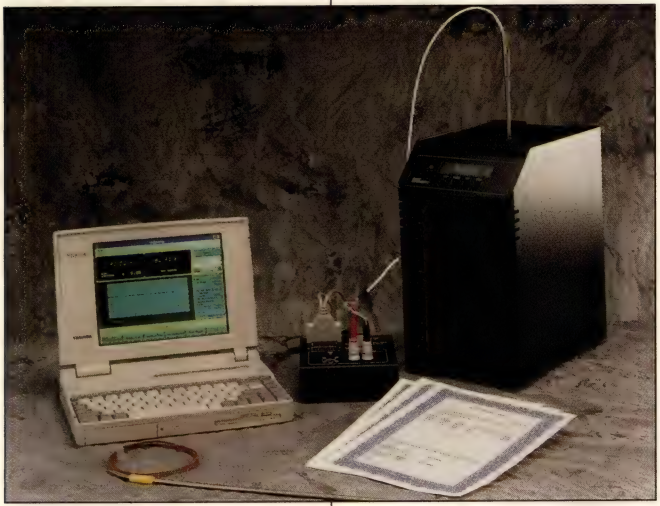
CIRCLE NO. 101

INDUSTRIAL ELECTRONICS SHOWCASE

PID CONTROL ALGORITHMS ADDED TO LABVIEW AND LABWINDOWS.

The LabView and LabWindows PID control packages include functions for P, PI, and PID algorithms; PID with external reset feedback; lead/lag compensation; automatic/manual control mode; error-squared PID; PID parameter tuning; and setpoint ramp/rest function. $295. **National Instruments**, Austin, TX. (800) 433-3488. **Circle No. 410**



▲SOFTWARE TO CALIBRATE RTDS, THERMOCOUPLES FROM –25 TO +600°C.

The 9931 Individual Sensor Calibration System software package automates the certification of a thermocouple or RTD from –25 to +600°C. It uses Hart Dry-Well Calibrators and a PC to make sensor calibrations. Readings are taken automatically after user-selectable stability has been reached. An interface thermometer reads thermocouple J, K, T, E, R, S, and B thermocouples; and it reads 100 Platinum; 385 and 392 Alpha; and 3- or 4-wire RTD types. The 9931 runs under Windows, costs $1490, and is sold as an add-on to the company's Dry-Well Calibrators. **Hart Scientific**, Pleasant Grove, UT. (801) 785-1600. **Circle No. 411**

DATA-ACQUISITION SOFTWARE SAVES 8 MILLION PRETRIGGERED DATA POINTS.

The new version of SnapMaster saves up to 8 million pre-triggered data points prior to a failure or catastrophe. The software's real-time plotting performance has increased sevenfold to 110,000 samples/sec. Other new features include button bars for frequently used commands and new graphical data displays for advanced data presentation. SnapMaster Version 3.0 required Windows or Windows for Workgroups v3.1 or higher, 4 Mbytes of RAM, and approximately 5 Mbytes of free disk space. The software's modules operate integrated or as stand-alone programs. The data-acquisiton module is $995, the general-analysis module is $495, and the frequency-domain module costs $495. **HEM Data Corp**, Southfield, MI. (810) 559-5607. **Circle No. 412**

DATA-ACQUISITION PACKAGE IS WINDOWS BASED.

Version 2.0 of WorkBench PC for Windows adds seven modules and many additional features. It will operate with most IEEE-488 boards and allows you to reset icons, display messages, and change icon parameters. Multiple displays are selectable by the keyboard or by user-specified trigger points. Automatic calibration increases accuracy for analog inputs and cold-junction sensors. The base edition, with 39 modules, is $995; the 49-module extended edition is $1246; a run-time edition is $329. **Strawberry Tree Inc**, Sunnyvale, CA. (408) 736-8800. **Circle No. 413**

MICROCONTROLLER ADDS 1 MBYTE OF ADDRESSING WITH CAN 2.0.

A new member of the MCO 96 microcontroller family, the 87C196CB, supports automotive and industrial applications. It features 1 Mbyte of external addressing and integrates the CAN 2.0 protocol specification. The device also includes 2 kbytes of on-chip RAM and a user-selectable 4× clock multiplier. In an 84-lead PLCC package, the 87C196CB costs approximately $19 (100,000). **Intel Corp**, Chandler, AZ. (602) 554-8080. **Circle No. 414**

REMOVABLE FLASH-MEMORY CARTRIDGES TOLERATE EXTREME CONDITIONS.

Targa's Series 1 removable flash-memory cartridges, with capacities from 10 to 250 Mbytes, operate in conditions too severe for disk drives. They withstand 30g shocks, 10g vibration (5 to 2000 Hz), altitudes to 50,000 ft, and temperatures from –40 to +85°C. They use little power, are noiseless, and have access times 20 times faster than disk drives. The cartridges fit Targa's Series 1 cartridge holders and data recorders, which are available with SCSI, serial, and parallel interfaces. The cartridge holders have the same form factor as a 5.25-in. disk drive. A 250-Mbyte cartridge sells for $8400 in OEM quantities. **Targa Electronics Systems Inc**, San Ramon, CA. (510) 277-0188. **Circle No. 415**

RUGGED, HANDHELD TERMINAL IS PROGRAMMABLE IN C.

The ST/2000P handheld terminal is programmable in C and features flexible memory choices for custom applications. The terminal's LCD can display 4 lines of 20 alphanumeric characters or 8 lines of 26 graphics characters. It can have as much as 256 kbytes of erasable flash memory and 512 kbytes of nonvolatile RAM. For fixed programs, 256 kbytes of EPROM can replace the flash memory. A real-time clock is optional. Lexan packaging enables the terminal to withstand repeated drops to concrete and to resist liquids. An optional protective rubber boot increases ruggedness still more, and optional extended-temperature components

extend operating-temperature range. The basic model costs $470 **WPI Termiflex Inc**, Merrimack, NH. (603) 424-3700. **Circle No. 416**

RUGGED PC-104 COMPUTER BOASTS GUIDED-ACOUSTIC-WAVE TOUCHSCREEN.

The 486-based Display-Pac104-SVGA flat-panel computer features both an 800×600-pixel active-matrix color LCD and a guided-acoustic-wave touchscreen. The touchscreen, an improvement over those using surface-acoustic-wave technology, uses ultrasonic waves dispersed through a thin piece of glass. It provides 92% optical clarity, 150 points-per-inch resolution, and pressure-senstive (Z-axis) control. The glass screen resists scratching and chemicals, and touchscreen operation is unaffected by materials that might collect on the screen's surface. Rigid metal packaging makes the system suitable for high-vibration environments. Together, the computer and display measure 12.6×8.6×3 inches. The backlit LCD measures 10.4 in. diagonally. Processor choices include 50-, 66-, and 100-MHz 486-type µPs. System price for the 50-MHz version is $6367 (25). **Computer Dynamics**, Greer, SC. (803) 877-8700. **Circle No. 417**

SOLID-STATE MODULE EMULATES DISK DRIVE.

The I2596 solid-state storage module provides as much as 96 Mbytes of nonvolatile, disk-emulating, NAND flash memory for use in harsh environments, including temperatures from 0 to 70°C. Measuring 4.00×2.75×0.76 in., the module is a plug-in replacement for a standard 2.5-in. IDE disk drive. It provides random access times of 0.3 msec and maintains sustained read transfers of 2.5 Mbytes/sec. Write speed is at least 250 kbytes/sec. IDE error correction and a proprietary flash-memory remapping algorithm combine to provide a module MTBF of 600,000 hours. 12-Mbyte module, $1177; 96-Mbyte version, $5295. **MemTech**, Sunnyvale, CA. (408) 745-1600. **Circle No. 418**

ST
TD300IN
F994A9427
D300I
91E435

TRIPLE IGBT/MOS DRIVER INCLUDES ALL INTERFACE FUNCTIONS.

The TD300 is a triple IGBT/MOS driver IC that integrates all the functions required to drive up to three power MOSFETs or IGBTs from CMOS or LSTTL logic signals. The device is suitable for a variety of motor-driving, power-switching, and high-voltage level-shifting applications. It includes an undervoltage lockout circuit, a current-sense comparator with an alarm output, enhanced latch-up immunity, and an op amp that can be used to interface the current-sense resistor to an ADC. The TD300IN and TD300ID cost $0.92 and $0.91 (5000), respectively. **SGS-Thomson Microelectronics**, Lincoln, MA. (617) 259-0300. **Circle No. 419**

VMEBUS CPU BOARD INCLUDES COMMUNICATION CONTROLLER.

The Nitro240/260 VMEbus CPU board includes a communications subsystem for applications that require a combination of high-speed computing, I/O, and data movement. The communications subsystem incorporates Motorola's MC68030 QUICC chip, which uses a 32-bit, RISC-based communications processor module to implement user-selected protocols and to manage seven serial channels, 16 DMA channels, and four independent baud-rate generators. The Nitro240/260 has a VME64 interface, an 80-Mbyte/sec Corebus mezzanine/local-bus interface, Ethernet and SCSI-II interfaces with DMA, and two serial I/O ports. Software support for the board includes VxWorks, pSOS+, and OS-9 operating systems. A 33-MHz Nitro240 with 8 Mbytes of DRAM costs $5195; a 50/66-MHz, 8-Mbyte Nitro260 is $5695. **Heurikon Corp**, Madison, WI. (608) 831-5500. **Circle No. 420**

24-BIT DSP FOR CONTROL APPLICATIONS.

The DSP56005 features an expanded on-chip program memory, a PWM peripheral, a watchdog timer, and a peripheral select pin. The expanded 4608-word program RAM allows eight times the code to run directly on chip without incurring wait states. This feature allows additional and more complex DSP algorithms, such as sophisticated control structures, to run more quickly. The 50-MHz DSP comes in a 144-pin thin quad flatpack for $50.70 (1000). **Motorola Inc**, Microcontroller Technologies Group, Austin, TX. (512) 891-2030. **Circle No. 421**

PCI MEZZANINE CARD ADDS VIDEO TO STD 32 SYSTEMS.

The zPM10 CompactPCI Super VGA Mezzanine Adapter adds 32-bit, 33-MHz video capabilities to Ziatech's Pentium-based STD 32 industrial computers. Based on Cirrus Logic's GD5434 VGA controller, the zPM10 provides as many as 16.8 million colors and displays with as many as 1280×1024 pixels. It's available with 2 Mbytes (standard) or 4 Mbytes of video memory and with an optional VESA feature connector for pass-through applications. Video-select circuitry allows as many as seven Pentium/PCI pairs to share a common monitor and keyboard. The card adheres to the mezzanine portion of the new CompactPCI specification of the PCI Industrial Computer Manufacturers' Group (PICMG). $425. **Ziatech Corp**, San Luis Obispo, CA. (805) 541-0488. **Circle No. 422**

TOUCH COMPUTER WORKS IN HAZARDOUS LOCATIONS.

The ErgoTouch Computer HL meets CSA Class 1 Division 2 requirements for operation in hazardous areas and is designed to withstand shock, vibration, humidity, and dust. It operates from 0 to 50°C, and all exterior surfaces are chemical resistant. The 486-based system is free standing and self-contained, requiring no purging or pressurization enclosures. You can also mount the 13.5×16.4×4.5-in. unit for integration with other equipment. The system comes with 8 Mbytes of RAM and a 262-Mbyte hard disk. The 640×480-pixel, 10.4-in. (diagonal) VGA flat-panel display provides 265 colors. $12,200. **Dynapro**, New Westminster, BC, Canada. (604) 521-3962. **Circle No. 423**

RAIL-TO-RAIL OP AMPS FOR AUTOMOTIVE APPLICATIONS.

The LMC6492 and LMC-6494 operate over –40 to +125°C while maintaining rail-to-rail input and output swing. Also for use in portable and low-power applications, the devices operate in applications from 5 to 15V, using an ultralow input current of 200 pA max. In an 8-pin DIP, the LMC-6492 costs $1.25 (1000); in a 14-pin DIP, the LMC6494 costs $2.05 (1000). **National Semiconductor Corp**, Santa Clara, CA. (800) 272-9959.

Circle No. 424

3V SILICON TEMPERATURE SENSOR.

The AD22103, the first silicon 3V-based temperature sensor, is guaranteed to exhibit accuracy better than 2°C and nonlinearity better than 0.5% over 0 to 100°C. It allows for high gain (28 mV/°C) and direct connection to standard ADCs and requires no additional signal-conditioning circuitry or linearity compensation. Housed in a TO-92 or SO-8 package, the sensor is suited for temperature monitoring in computers, cellular and cordless phones, and other portable and low-power equipment. It costs $0.98 (1000). **Analog Devices**, Canton, MA. (617) 937-1428.

Circle No. 425

12-BIT APPLICATION-SPECIFIC SAMPLING ADC TARGETS ELECTRONIC IMAGING.

The 12-bit, 2-MHz ADS-CCD1202 delivers 600 μV rms and differential linearity error of ±0.45 LSB max. It operates from one 5V supply or either ±15 or ±12V supplies, and it consumes a maximum of 1.95W. Applications for the edge-triggered ADC include photo-CD image capture, medical diagnostic imaging, and infrared imaging. The ADS-CCD1202MC, which operates over 0 to 70°C, costs $199 (100). The ADCCD-1202MM, which operates over –55 to +125°C, costs $264 (100). **Datel Inc**, Mansfield, MA. (508) 339-3000.

Circle No. 426

8-BIT FLASH ADC GUARANTEED UP TO 1 GSAMPLE/SEC.

The SPT7760, a monolithic, 8-bit ADC, has an analog input bandwidth of over 900 MHz. With its sample rate of 1 Gsample/sec, the device suits A/D-conversion applications in digital scopes, transient capture, radar, and electronic counter measures. It has a low input capacitance of 15 pF and comes in a 68-lead pin grid array and an 80-lead surface-mount MQUAD package. From $590 (100). **Signal Processing Technologies**, Colorado Springs, CO. (719) 528-2314.

Circle No. 427

NEW DMMS EXPAND TEKTOOLS LINE.

The $595 TekWaveMeter THM 420 is a handheld digital multimeter with graphical waveform display for troubleshooting, maintenance, installation, calibration, and repair of electronic equipment. The penmeter-form-factor $59 DMM 150 features an analog bar graph, auto power off, continuity beeper, data hold, diode test, and range hold. The full-featured DMM 247 and 249 autoranging DMMs are dust- and water-resistant; they cost $145 and $185, respectively. **Tektronix Inc**, Beaverton, OR. (800) 426-2200.

Circle No. 428

IN-VEHICLE DATA-ACQUISITION AND TESTING SYSTEM.

The Drive portable turnkey automobile data-acquisition system incorporates LabView, operates on 12V dc, and lets you acquire data from a moving vehicle under test-track or over-the-road test conditions. LabView's graphical user interface lets you configure and recall test setups, including channels, gains, displays, and file I/O. The 16×16×8-in. system contains a Dolch 486 66-MHz computer with 32 Mbytes of RAM, a 532-Mbyte hard drive, and a color monitor; a workstation version has a 75- or 100-MHz 486 processor, 16 Mbytes of RAM, a 520-Mbyte hard drive, and a color monitor. From $25,000. **Dateppli**, Midland, MI. (517) 839-1040.

Circle No. 429

PORTABLE DATA-ACQUISITION SYSTEM FOR HARSH ENVIRONMENTS.

The Field PC is available as a stand-alone portable PC or with data-acquisition boards and software integrated into one rugged system. Standard features include a 75-MHz 486 IBM Blue Lightning processor; shock and vibration-dampening system; three full-size AT/XT slots or six IBM open-standard ISA expansion half slots; integrated PCMCIA-card expansion slot; 12V dc power input; and 8 Mbytes of RAM. The Field PC FWS costs $9869; and Field PC FWS 7501 (includes 520-Mbyte hard drive) costs $10,699. **Keithley MetraByte**, Taunton, MA. (800) 348-0033.

Circle No. 430

MULTI-INPUT UNIT FOR DATA ACQUISITION.

The 9040 MIU is a compact data-acquisition unit with modular construction for measuring up to 24 signals from a variety of sensors and transducers. It can be configured to read any combination of all-media pressures, thermocouples, RTDs, and other inputs ranging from ±10 mV through ±10V. It consists of a common chassis, up to eight Model 9044/9045 analog plug-in input blocks, and an optional frequency input block. From $2500. Delivery, eight weeks ARO. **Pressure Systems Inc**, Hampton, VA. (800) 678-7226.

Circle No. 431

10-MHZ ARBITRARY-WAVEFORM BOARD FOR PC/ATS FEATURES WINDOWS VIRTUAL-INSTRUMENT SOFTWARE.

The PC-420 high-speed arbitrary-waveform-generator board uses digital synthesis to generate two simultaneous analog outputs up to 10 MHz. It also features a sample update rate to 40 MHz, a high-resolution frequency-synthesized clock, software-programmable offset and gain, and external clock, trigger, and gate inputs. It measures 4.5×13.3×0.5 in. and costs $1495; the PC420GEN Windows virtual instrument software costs $95 (executables only) or $395 for the PC420SRC Visual Basic and C source code. **Datel Inc**, Mansfield, MA. (508) 339-3000.

Circle No. 432

LINEAR-ACTIVE FILTERS HAVE –100-DB ATTENUATION.

The D68, 828, and 858 fixed-frequency and programmable filters suit use in anti-alias-filtering, data-ac-quisition, communication, medical, aerospace, navigation, and sonar applications. Lowpass filters include Butterworth, Bessel, elliptic, and constant-delay transfer functions. Butterworth and elliptic filter are also available in highpass versions.

The devices have profiles as low as 0.30 in. Fixed-frequency models have factory-set corner frequencies of 10 Hz to 100 kHz, and 8-bit models are programmable from 1 Hz to 102.4 kHz. The fixed-frequency D68 costs $151 (1) or $120 (1000); digitally programmable models 828 and 858 cost $410 and $385 (1), respectively, or $295 and $275 (100), respectively. **Frequency Devices Inc**, Haverhill, MA. (800) 252-7074. **Circle No. 433**

THIN-FILM RESISTORS SUIT PENTIUM P6.

The IPEC RG series of thin-film resistors suits use in Pentium P5 and P6, PowerPC, and RISC-processor applications. The devices integrate 22 resistors in a 25-mil QSOP and feature center-placed ground pins to reduce ground-bounce effects and achieve low lead inductance. The resistors can directly replace multilayer ceramic resistor chips and thick-film surface-mounted packaged networks. $0.95 (10,000). **California Micro Devices Corp**, Milpitas, CA. (408) 263-3214. **Circle No. 434**

STAINLESS-STEEL SENSOR SUITS HARSH-DUTY SENSING.

The Series 976 two-wire, stainless-steel proximity sensor can be wired to current-sink or current-source configurations and can interface to all standard PLCs. The devices feature low leakage current and reverse-polarity, transient/ false-pulse, and short-circuit/ overload protection. Typical applications include factory automation, machine tools, transfer lines, food-processing equipment, parts positioning, and presence/absence sensing. The devices come in 12-, 18-, and 30-mm sizes with prices starting at $115, $120, and $125, respectively. **Honeywell Inc, Micro Switch Division**, Freeport, IL. (800) 537-6945. **Circle No. 435**

POWER TRANSFORMERS HAVE LOW PROFILE.

The SPW-2100 series of power transformers measures 2 in. long×1.562 in. wide×0.900 in. high typ. The devices are rated at 6 VA and have outputs from 5 to 230V ac. $4. **PREM Magnetics Inc**, McHenry, IL. (815) 385-2700. **Circle No. 436**

MINIATURE CURRENT TRANSFORMER IS LINEAR OVER 10,000-TO-1 RANGE.

This addition to the Mini-CT line of miniature current transformers offers a 10-μA to 20A input current with nominal output of 0 to 2V. The device is linear over a 10,000-to-1 range, eliminating the need for multiple sensors and sensor switching. The transformers come in five decades of linear response and provide 40-Hz to 10-kHz bandwidth and 5% accuracy. Units are available with nominal ratings of 5, 10, and 20A. $5. **Amecon Inc**, Anaheim, CA. (714) 634-2220. **Circle No. 437**

DC/DC CONVERTERS FOR EXTREME ENVIRONMENTS.

This family of 50W power supplies offers stable power conversion in harsh environments without the need for additional engineering or external components. The devices are available in single, dual, or triple outputs and integrate transient suppression, input and output filtering, control and monitoring, heat sink, and shock and vibration immunity in a rack- or chassis-mountable package. Six voltage ranges are available from 8 to 35V dc. Prices start at $425 (25). **Melcher Inc**, Chelmsford, MA. (508) 256-1812. **Circle No. 438**

DIGITALLY COMPENSATED PRESSURE TRANSDUCER.

The P4100 series of digitally compensated pressure transducers is available in 0- to 5-psi to 0- to 10,000-psi pressure ranges. The transducers provide ±0.1% full-scale output max and <0.0125%/°C combined thermal error over a –25 to +85°C temperature range. Prices start at $289. **Lucas Control System Products, NovaSensor**, Fremont, CA. (510) 490-9100. **Circle No. 439**

GATE-DRIVE TRANSFORMERS FOR MOSFET SWITCHING SUPPLIES.

The GDT series of gate-drive transformers provide fast rise times for switching frequencies >100 kHz. The drivers have three insulating barriers from primary to secondary and 4200V-rms withstanding capability. The devices provide two fully floating outputs, each with a 1-to-1 turns ratio with respect to input. Three models offer 25-, 50-, or 100-kHz operating frequency, respectively, and all withstand –40 to +130C° operating temperature. Leakage inductance is <1% typ. The GDTO25100, GDT50100, and GDT100 100 cost $2.70, $2.03, and $1.82 (1000), respectively. **GFS Manufacturing Co Inc**, Dover, NH. (603) 742-4375. **Circle No. 440**

HALL-EFFECT SENSOR IS TEMPERATURE-COMPENSATED.

The temperature-compensated SS100 series Hall-effect position sensors operate from the magnetic field from a permanent magnet or electromagnet. Typical

The Port Authority.

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A series of 6A subminiature pushbutton switches fits standard 22-mm panel cutouts. The devices inhibits sparking and increases operating life in ac circuits. Single-, double-, and 4-pole switches are available with either momentary or alternate action circuits. Models with silver terminals rate at 6A at 124V ac and 3A at 250V ac. The gold-plated terminals rate at 0.4 VA max at 28V ac/dc max. $8.90 (100). **NKK Switches**, Scottsdale, AZ. (602) 991-0942.

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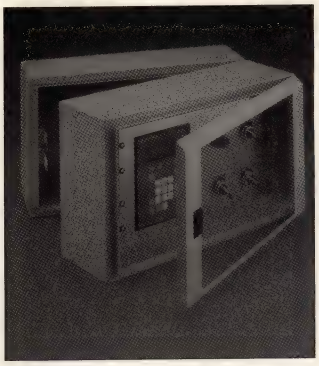

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70V dc ranges and the universal ac ranges. The input ranges are designed for supplying power in mobile or remote applications. Output is over the entire range. Undervoltage and overvoltage lockout ensure that full power is available when the input voltage is within the specified 5:1 range. Prices start at $552 (100). **Melcher Inc**, Chelmsford, MA. (508) 256-1812.

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CIRCULAR CONNECTOR FOR INDUSTRIAL APPLICATIONS.

This series of MIL-C-5015 style connectors range in size from three to 19 contacts. The connectors are suited for applications that require protection from moisture, oil, and dust. Each device contains a premating grounding contact that is designed to mate before the current-carrying contacts and protect the user against shock. $30/mated pair (100) for a four-position device. **DDK Electronics Inc**, San Jose, CA. (408) 980-8344.

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This family of 50W power supplies offers stable power conversion in harsh environments without the need for additional engineering or external components. The devices are available in single, dual, or triple outputs and integrate transient suppression, input and output filtering, control and monitoring, heat sink, and shock and vibration immunity in a rack- or chassis-mountable package. Six voltage ranges are available starting at 8 to 35V dc. Prices start at $425 (25). **Melcher Inc**, Chelmsford, MA. (508) 256-1812.

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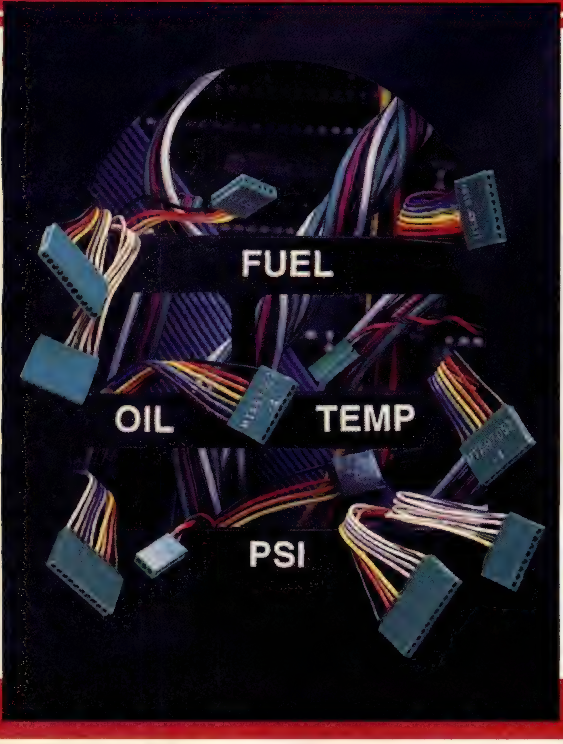

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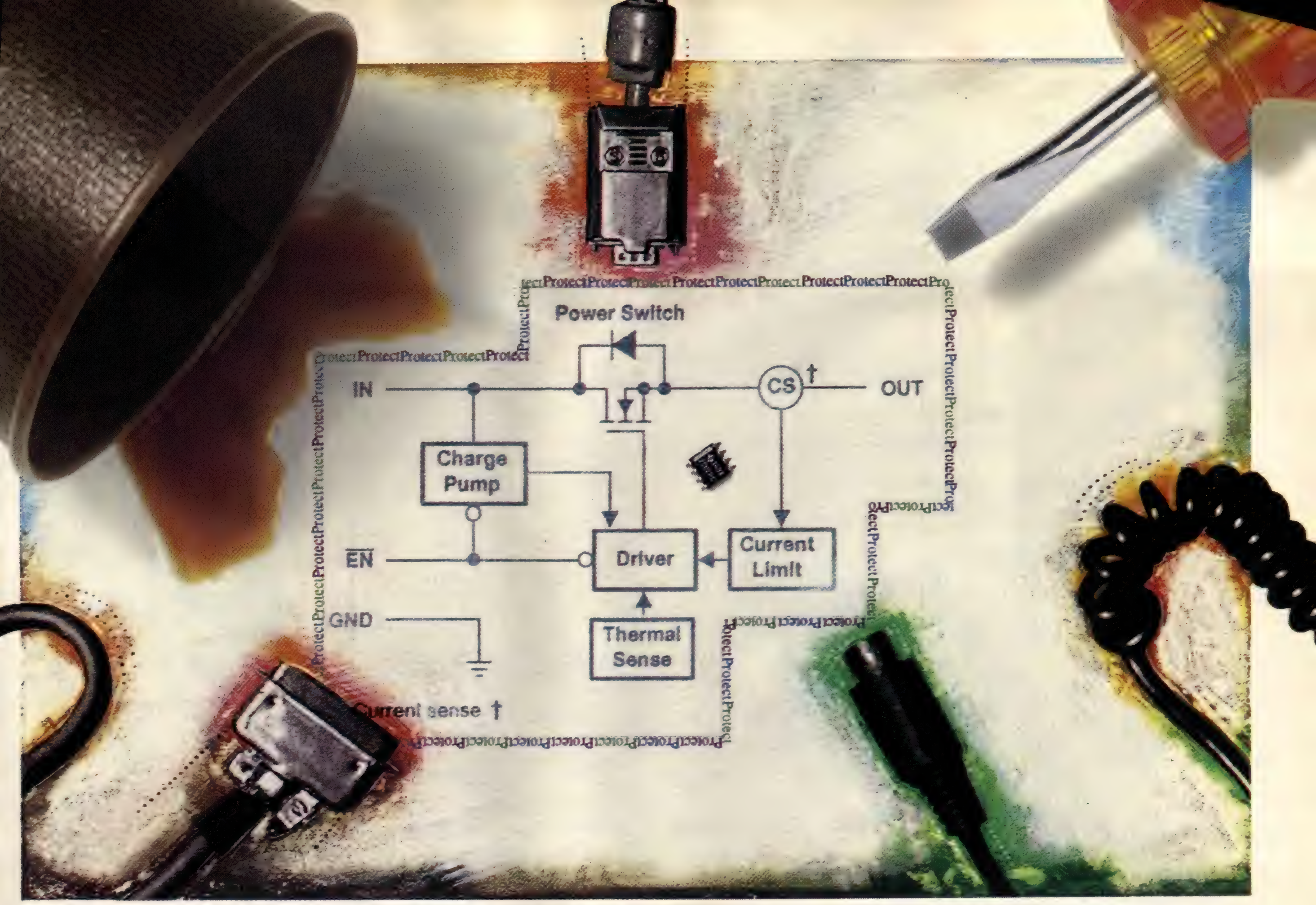

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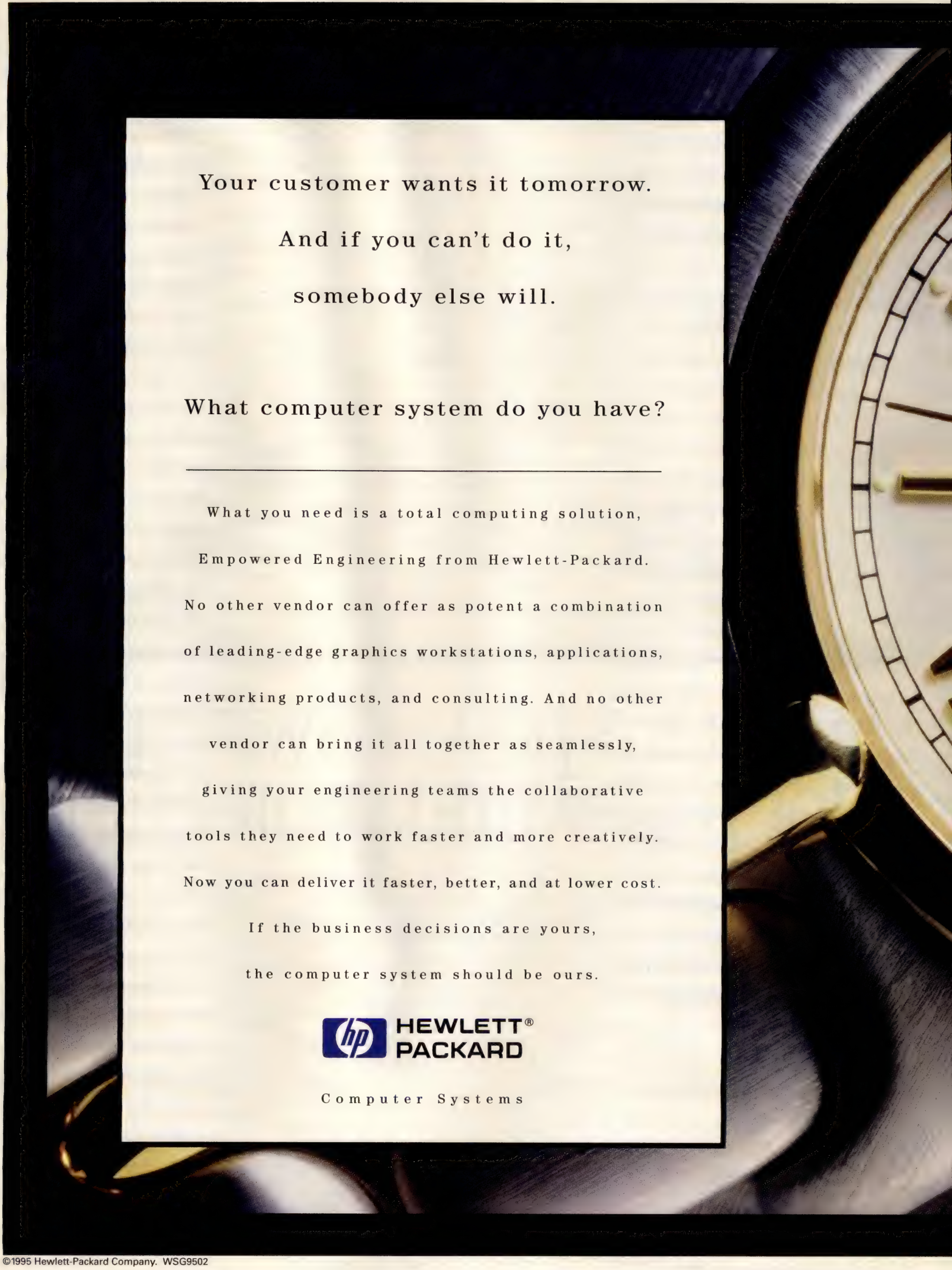

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MISSION-CRITICAL COMPUTING

WHEN COMPUTERS must not fail...

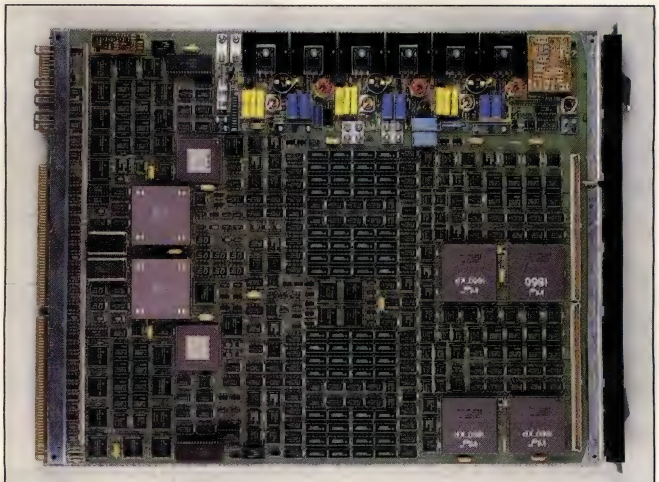
INDUSTRIAL ISSUE

When a computer failure can take down an industrial process or a whole company, computer systems that keep running command high prices. Newer software and hardware are cutting the price premium, though—and none too soon; demand is exploding for computers that just won't quit.

DAN STRASSBERG,
SENIOR TECHNICAL EDITOR

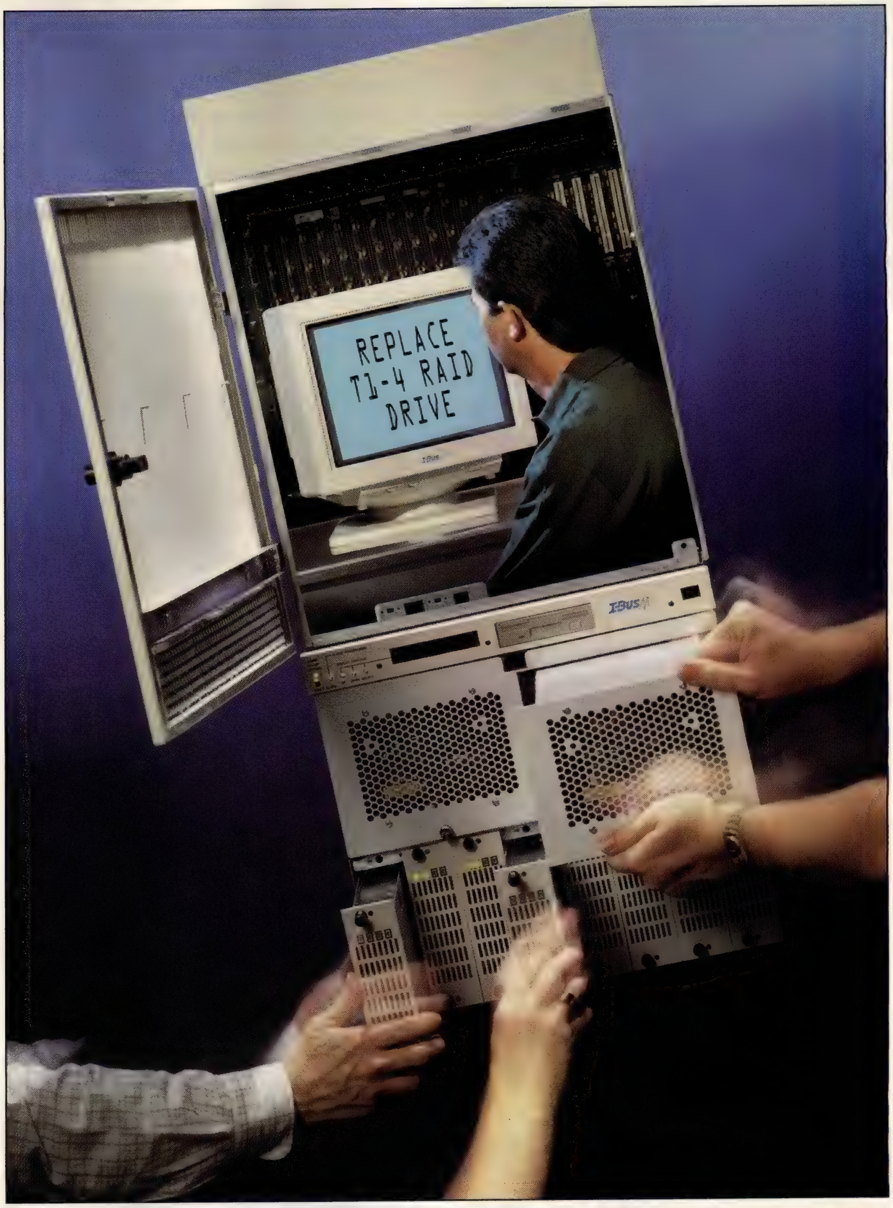
Some computer systems simply *must* not fail. More and more, computers that handle real-time industrial applications have to stay on-line at all times. At present, the Holy Grail of computer-system uptime is "five nines" (99.999%) availability—about five minutes of downtime per year. Because not all mission-critical applications need or can afford such low downtime, many ways to increase uptime have emerged. Although most schemes use special hardware, software figures at least as strongly in preventing and recovering from system crashes. Within certain limits, software now makes it possible to build fault-tolerant systems from standard workstations and PCs.

Suppliers of so-called fault-tolerant or continuous-availability products like to focus on uptime. Although this orientation puts a positive spin on downtime, it can obscure major differences among products. Availability of 99.9% *sounds* a lot like 99.99%. But a system that delivers 99.99% availability is 10 times as reliable as one that offers 99.9% and usually commands a higher price. A less expensive class of products goes by



This processor board from Stratus includes twin dual-processor CPUs (lower right and center right), twin bus-interface ASICs (center left), and duplicate buses (far left). The connectors at the far right are twin logic-analyzer interfaces used in test. Newer versions supplant these two connectors with IEEE-1149.1 boundary-scan ports.

Photograph courtesy I-Bus ▶



This high-availability industrial PC is configured for telecommunications applications. Note the redundant power supplies near the bottom, the RAID just below them, and the passive PC backplane near the top.

the name "high availability." Few products that go by this name have been around long enough to establish track records for reliability. Thus, in the high-availability area, vendors focus on features that enhance systems' reliability.

Manufacturers of hardware-based fault-tolerant systems (IMP, Sequoia, Stratus, and Tandem, for example) do quantify uptime. These companies have supplied continuous-availability products for at least a decade. These systems' primary applications are in telecommunications and on-line transaction processing (OLTP). Airline-reservation and brokerage systems are two examples. Prices start at under $100,000, although configurations that cost from $200,000 to $500,000 are more common. Before paying such prices, customers must calculate a payback, and documented reliability is essential for the calculations.

However, you don't need to spend $100,000—or even half as much—to obtain reliability far greater than that of standard workstations and PCs. Several vendors of industrial PCs and VMEbus products (see **box,** "For free information...") offer systems that duplicate the hardware elements that are most likely to fail—power supplies, hard disks, and blowers. Some systems also continuously monitor key indicators of impending failure, such as power-supply voltages, airflow, air temperature, and fan rotation. These systems warn operators of conditions that can foretell failures. Thus, high-availability industrial PCs provide a measure of fault tolerance at a fraction of the cost of true continuous-availability systems.

Hot swapping of key system elements is another feature of some of these PC and VMEbus products. A hot-swappable system element is one that you can unplug or install without powering the system down and, ideally, without disturbing system operation. In addition to many hard-disk drives used in RAIDs (**Ref 1**), the components that are currently farthest along in hot-swappability are power supplies and fans.

Hot-swappable I/O controllers and CPUs—standard features of true fault-tolerant systems—are virtually nonexistent in PCs. You can buy VMEbus products that permit hot swapping, however. Currently, you achieve hot swapping of VME boards by using interposers—short extenders that fit between standard VME boards and the backplane. The VME-64 bus, whose specification is currently under review pending ratification, will eliminate interposers.

VME-64 provides hot swappability as a standard feature, thanks in part to special five-row DIN connectors supplied by Harting Elektronik. The connectors assure that ground connections are the first made and the last broken when you insert or remove a board. Specially developed bus-interface ICs safeguard against "glitching" the bus with transients when you insert or remove a board. The ICs, currently available from Texas Instruments as the ETL series, will also be available from National Semiconductor.

Another feature of these ICs is incident-wave switching. This feature increases the bus speed by assuring that signals cross logic thresholds immediately as they propagate down the bus. Older technology required a signal reflection from the end of the bus to bring the voltage level above the threshold.

Despite their interest in high-availability computing, some manufacturers of industrial PCs and VMEbus products question how soon (or even whether) the documented low downtime of continuously available OLTP systems will come to industrial applications. The reason is that typical industrial systems dedicate a high percentage of their hardware to handling real-time I/O.

Although OLTP systems also handle lots of I/O, the nature of the I/O devices is different. Operator terminals are the most common I/O devices in OLTP. In industrial applications, contact closures, ADCs, and DACs are the most common. Whereas duplicating these system elements is technically feasible, wiring complexities and cost have deterred manufacturers from offering redundant real-time I/O hardware.

Not everyone thinks fault-tolerant computing is impractical for areas such as factory automation, however. For example, Isis Distributed Systems supplies software tools for creating fault-tolerant applications that run on networks of standard workstations. The company points with pride to a new Advanced Micro Devices wafer-fab facility as a showcase for the advantages of using Isis' tools to develop manufacturing-control applications.

Saying that software plays a key role in system availability is a clear understatement. Whereas every high- and continuous-availability system depends on redundant hardware in some form, software problems can bring the most sophisticated hardware to a dead stop.

Although vendors of fault-tolerant hardware address many potential software problems in their operating-system (OS) software, a new type of software tool aims at creating systems that survive an even wider range of faults. These tools create continuously available systems by networking standard workstations and PCs. Because such networks use mass-produced hardware, they can be less expensive than systems based on specialized hardware. (The networks are more expensive than non-fault-tolerant and even high-availability approaches, however.) In general, too, these networks take longer to recover from faults than systems based on hardware fault tolerance.

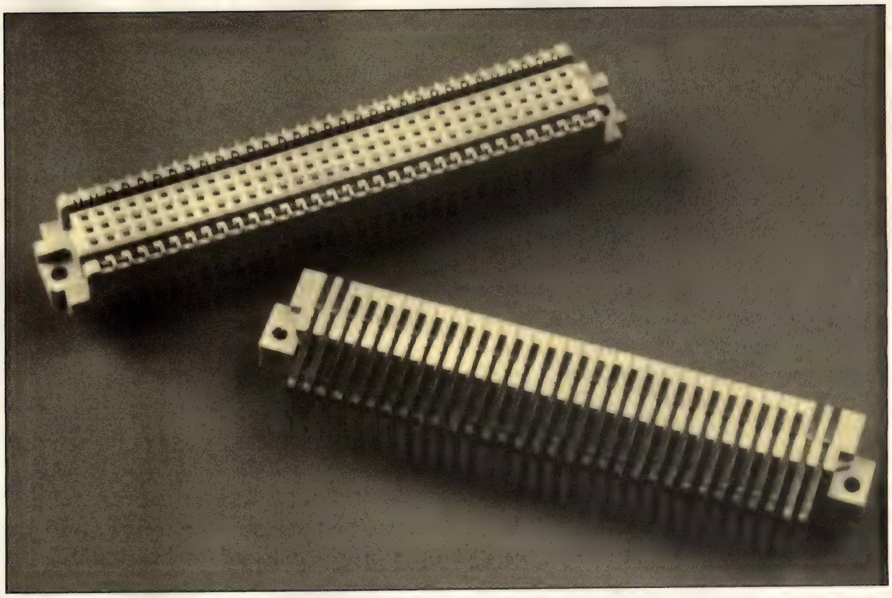
By placing interposer boards, such as this Vero Electronics live-insertion module, between standard VMEbus boards and a VME backplane, you can remove and insert the boards without powering down the system.

As with more conventional fault-tolerant systems (ones with tightly coupled redundant hardware elements), the objective of fault-tolerant networks is to eliminate single points of failure (SPFs). When viewed in the proper light, groups of standard workstations running specialized software that synchronizes communication among the group members contain no SPFs.

"Synchronizes" isn't a totally accurate term because fault-tolerant networks don't require messages to arrive at all destinations simultaneously. Synchrony in a fault-tolerant group of networked computers requires that no group member act on any message until it knows that the message has reached all members. Each group member must acknowledge to its peers within a specified period that it has received a message. If group members can't confirm that some member has received a message, they isolate the suspect member, divide its tasks among themselves, and roll back the image of system activity that each maintains to what existed when all group members last functioned normally.

In theory, the group members can be widely dispersed geographically; they might even communicate via the Internet. (A group linked by the Internet would not operate in anything even remotely resembling real time, however.) In practice, the group members are rarely more than a few miles apart. Even then, system architects make sure that group members share as few system elements as possible. For example, group members receive ac power from different ac mains (though usually from the same power company).

Many factors determine how rapidly such a networked group can recover (that is, resume more or less normal operation, even if not at full speed) from the failure of a member (where "member" includes a computer and its associated communications facilities). The speed of communication is espe-



The VME-64 bus will use this special five-row connector from Harting Elektronik. By ensuring that the ground connections are the first made and the last broken, the connector helps VME-64 to permit live insertion and removal of boards without the use of interposers.

cially important. Generally, recovery takes from several seconds to several minutes. Of greater importance, though, is that recovery—in the sense defined here—requires no human intervention.

In contrast, systems that base their fault tolerance mainly on specialized hardware often recover in nanoseconds. However, the types of failures from which hardware-based fault-tolerant systems can recover are somewhat limited. Hardware-based fault tolerance facilitates recovery from deterministic failures; fault tolerance based on message synchrony permits recovery from *any* kind of failure. Although deterministic problems include many software faults, certain software faults can bring down systems whose fault tolerance depends primarily on hardware. Computer scientists have named these faults Heisenbugs, after the Heisenberg uncertainty principle.

Heisenbugs are elusive faults that appear following particular, seemingly innocuous sequences of events. Because such faults are unpredictable, software engineers cannot eliminate them by design. One way that message-synchronized fault-tolerant networks keep nondeterministic bugs from causing serious problems is by dynamically allocating tasks among group members. The networks allocate tasks in a way that prevents the members from doing quite the same thing at the same time. For true fault tolerance, group members still must check each other's calculations. If results don't agree, the

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group must determine which result is correct and remove the member that caused the error from service.

Although the concepts of message-synchronized fault-tolerant networks are over a decade old, the networks were impractical until economical workstations that process multiple MIPS became available. Maintaining message synchrony requires a lot of computing power—one estimate is about 0.5 MIPS per computer. Unless each of the networked computers can process significantly more than 0.5 MIPS, inadequate power remains for the *real* computing tasks.

Isis Distributed Systems provides so-called middleware, which allows application developers to design fault-tolerant networked (client-server) applications with little concern for the impact of fault tolerance on their code. The Isis System Developers' Kits contain libraries of routines that developers bind into their code. These routines handle message synchronization across the network. Development licenses start at $3000; runtime licenses start at $400.

Hardware-based fault-tolerant computing systems are among the most highly sophisticated and impressive computers that exist. Hardware developers are starting to ask whether the disease that these elegant products cure is becoming so rare that the cure is superfluous, however. With or without fault-tolerant designs, the reliability of computer hardware continues to improve steadily. Still, it's hard to imagine a responsible developer of a mission-critical application entrusting such an application to a single conventional workstation or PC.

In general, systems based on hardware fault tolerance include at least two of every major element. Surprisingly, though, some fault-tolerant systems use fewer than twice the number of hard-disk drives that an otherwise-equivalent non-fault-tolerant system would use. RAIDs that contain five or nine drives (vs four or eight for equal-capacity non-fault-tolerant configurations) are examples. Arrays that include redundant drives can correct errors caused by a failure of any single drive. Similarly, some systems use n+1-redundant power supplies. For example, if two supplies can provide all of the system's power needs, the system includes three units.

Although all true fault-tolerant computers contain at least two CPUs, most contain more. When there are just two CPUs, both make the same calculations and compare the results. If the results match, the system assumes all is well, and the work proceeds. If the results don't match, diagnostic routines determine which CPU has malfunctioned. IMP uses this approach. In IMP's implementation, the diagnostics have 100 msec to report a result. If a CPU fails to report its status in that time, the surviving CPU takes it off-line.

LOOKING AHEAD

Factors as seemingly unrelated as just-in-time manufacturing and the declining cost of electronic hardware are coming together to increase the importance and the practicality of nonstop computing. When customers depend on uninterrupted supplies of components and materials, the computers that control the production of those items had better not fail. At the same time, even nonstop-computing approaches that derive their fault tolerance from software use lots of powerful hardware. The declining cost of that hardware is bringing nonstop computing within reach of the companies that need it.

The digital-communications revolution also places increasing emphasis on nonstop computing. The distinction between computers and communication systems is already quite blurry. Whether the communication system is a central office or a fax server on a network, downtime is anathema. Computer-industry observers expect a new class of computer system—the communications computer—to emerge. Fault tolerance will be a hallmark of such systems.

IMP systems can also contain three CPUs. When one disagrees with the other two, the CPU that disagrees is assumed to be in error. Some systems from Tandem use a similar voting scheme. IMP's three-processor systems offer an additional advantage: If one of the three CPUs fails, the remaining two CPUs continue to provide fault tolerance. Although all true fault-tolerant systems continue operating after a failure, many cannot operate after a second failure until at least one of the failures is repaired.

Systems from Sequoia use two CPUs per computing element, but the number of computing elements varies. Sequoia's system software dynamically allocates tasks to the computing elements. If the two CPUs in an element disagree, the system takes the offending element off-line, redistributes the tasks among the remaining elements, and rolls back all elements' system-activity records to the point before the fault occurred. In systems that contain three or more computing elements, Sequoia's approach, like IMP's, results in continued fault tolerance despite multiple failures. Themis uses a similar approach. Some Themis systems run applications built with the aid of Isis tools.

Stratus systems also use two CPUs per computing element. Many Stratus CPUs contain multiple μPs, however. Systems contain two computing elements. The pair of CPUs within a computing element and the pair of computing elements in the system all run in lock step. (In other words, four CPUs run in lock step.) If the two CPUs in a computing element disagree, the computing element goes off-line before the error can propagate beyond the computing element. Hence, there is rarely a need to roll back the image of system activity, and there is no loss of computational power.

Attention to detail

Although the following discussion emphasizes features of Stratus' Continuum systems, the goal is not the promotion of Stratus over its competitors. The discussion appears because continuous-availability systems represent the

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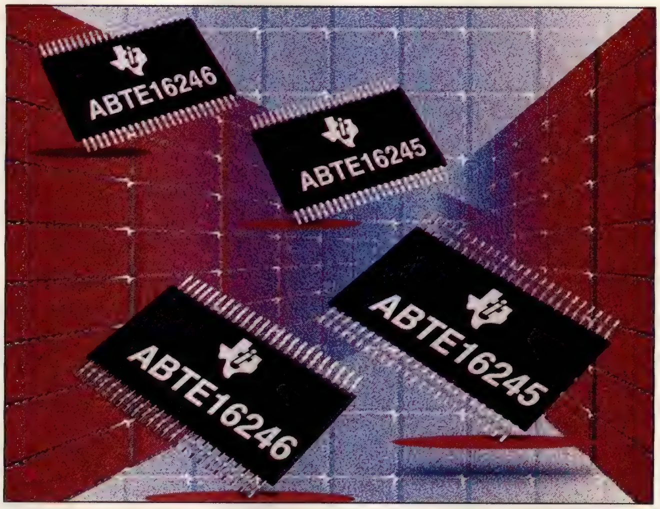
ultimate in commercial-product reliability. Although other vendors' systems differ from Stratus' in detail and even in major elements of design philosophy, the attention to detail is common to all. In your own application, you must decide how closely you need to approach the reliability of continuous-availability systems. Based on that appreciation, you should be able to decide how many of the concepts of continuous-availability systems your product must incorporate.



Enhanced-transceiver-logic (ETL) ICs from Texas Instruments are an enabling technology for the VME-64 bus's hot-swap capability. The ICs also implement incident-wave switching, which helps to speed bus transactions.

Fault-tolerant systems duplicate much more than the CPUs and computing elements. Other duplicate elements include memory and I/O buses, communication links, cooling fans, and peripheral controllers. (Note that using a RAID with a single disk controller does not safeguard against a controller failure.) Some vendors duplicate backplanes, although Stratus doesn't. All data transferred over buses include error-correction codes.

Stratus systems use mirrored hard-disk arrays (RAID level 1) but use only one mirrored-array pair per system. To achieve high transfer rates, the arrays use data striping. (That is, they divide the data accessed in single reads and writes among multiple drives that read and write simultaneously.) The drives use error correction internally, but the systems do not duplicate drives within either half of a mirrored-array pair. (In RAID terminology, the level-1 pair comprises two level-0 arrays.)

Besides constantly comparing the results of computations, Stratus systems continually execute diagnostic routines as background tasks. The routines are hard-coded into the CPU-board logic and, thus, do not directly involve the CPUs. The operating system is oblivious to the diagnostics; hence, the diagnostics don't cause Heisenbugs.

When a failure occurs, the system element that detects the failure

- immediately takes the offending element off-line to contain the failure,
- writes a diagnostic message into nonvolatile memory in the offending element, and
- dials the Stratus customer-assistance center, which arranges to ship a replacement module to the system site.

At the factory or field repair center, the diagnostic message aids the repair technician. The message also remains inside the failed module, even after repair, providing a lifelong indication of the unit's repair history.

The IEEE-1149.1 boundary-scan-testability standard figures heavily in Stratus' hardware architecture. For example, the system writes its diagnostic messages into nonvolatile RAM through the RAM chips' IEEE-1149.1 test-access ports (TAPs). Stratus design standards require that all digital ICs the company uses incorporate IEEE-1149.1. Designs that use noncompliant devices require the approval of a Stratus vice president.

Avoiding human error

Human error can defeat the best fault-tolerant design. Because most repairs to fault-tolerant systems are made by customer personnel while the systems remain on-line, Stratus and other companies use a series of red, yellow, and green LEDs to indicate module status. The LEDs guide relatively unskilled operators to replace the correct modules and, more important, not to remove modules that must remain in place. A green light signifies that you can remove a module. Pulling a module that displays a red light will cause the system to fail. A flashing yellow light indicates a module that has gone off-line because of a problem. A module that displays both green and yellow lights is, in effect, warming up.

Warm-up consists of the following steps: When you plug a module in, it first runs a group of self tests. Then, it synchronizes with the system clocks and copies the contents of all memory and registers from its counterpart. Copying goes on in the background while the counterpart module remains on-line. The copying process can take several minutes, during which the system performance may degrade somewhat.

Stratus systems use a distributed power architecture. Redundant bulk supplies with battery backup deliver loosely regulated 48V dc to the modules, each of which includes a pair of dc/dc converters. The bulk supplies receive power from separate ac mains through separate circuit breakers and power switches. The separate switches prevent operators from taking a system off-line by inadvertently powering it down. Within the modules, each CPU in a computing element has its own dc/dc converter.

Like systems that offer mere high availability, Stratus systems monitor reliability-related functions, such as airflow, temperature, and supply voltages. Unlike some high-availability systems, though, these continuous-availability systems do not involve the main

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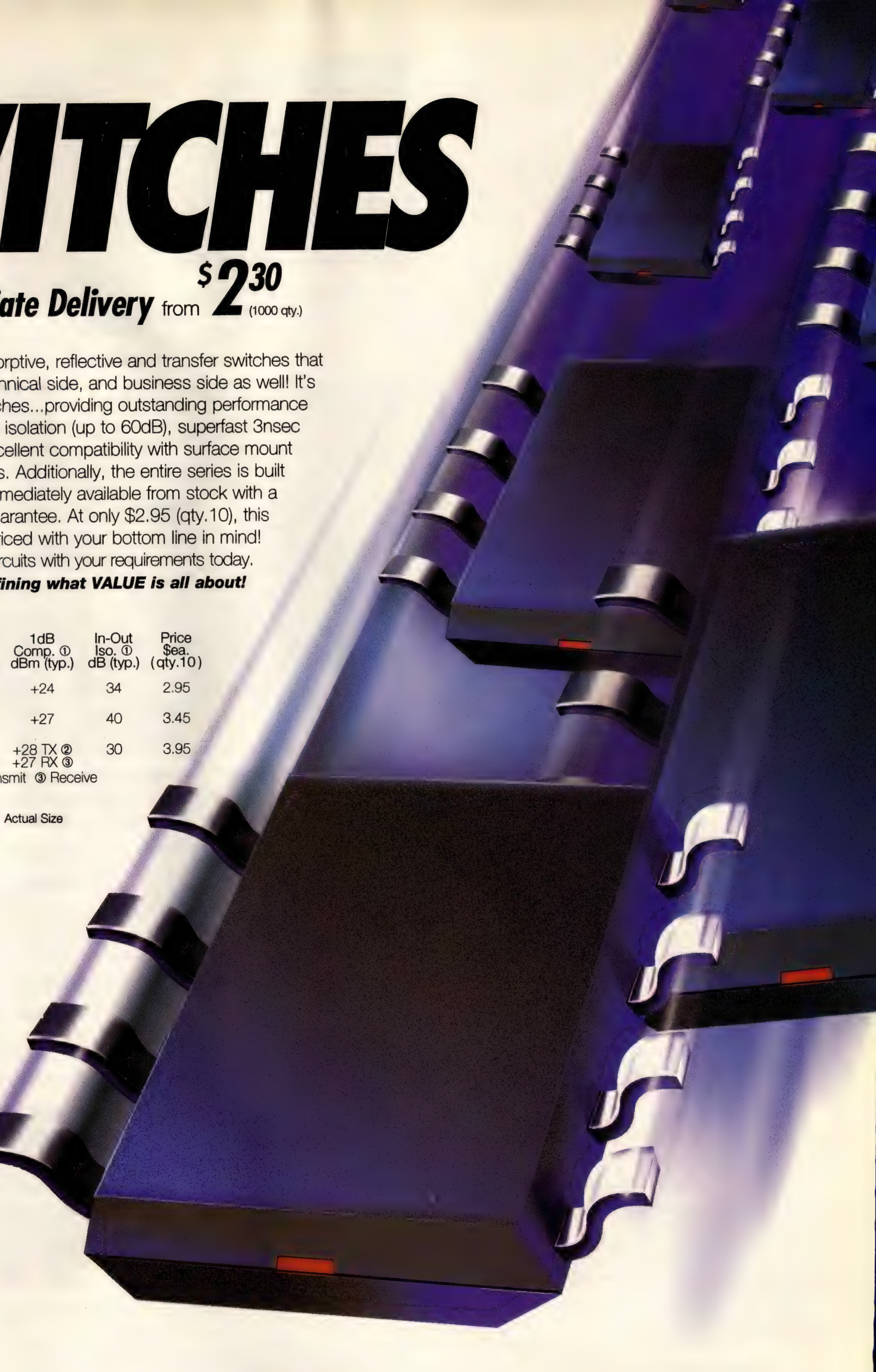

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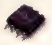

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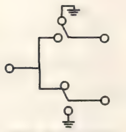

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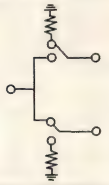

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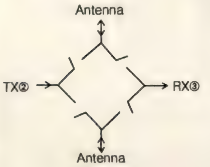

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processors in such mundane tasks. Instead, dedicated maintenance processors handle these low-level chores.

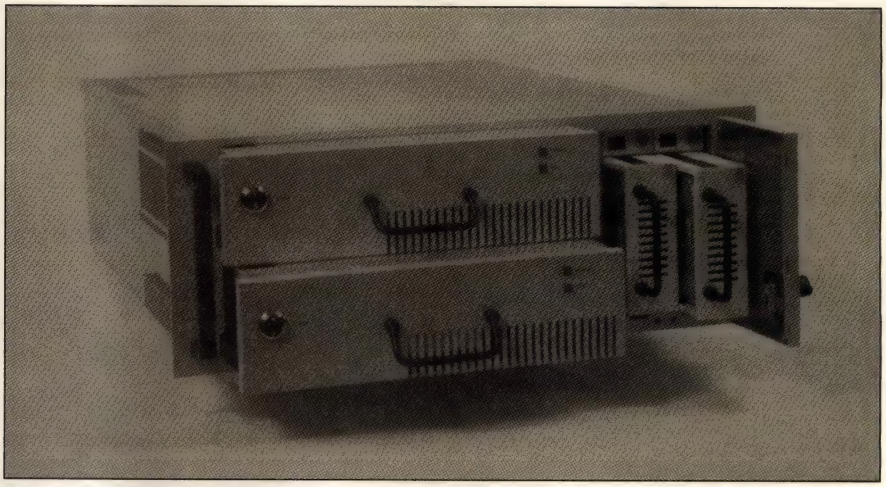
Some of Stratus' hot-swapping features resemble those of VME-64. When you insert or remove modules, special connectors assure that the ground connections are the first made and the last broken. Bus drivers remain in a high-output-impedance state until a module is ready to transmit data. Line receivers do not accept data from the bus until the module has successfully run diagnostics. Shorting adjacent backplane pins does not affect system operation. If you observe the red lights, the only effect of inserting and removing modules is a slight throughput degradation as replacement modules copy information from modules that are on-line.

Contain those faults

Stratus hardware emphasizes fault containment—keeping faults from propagating beyond the element in which they first appear. So, too, does the company's OS software. The company's original systems used a proprietary OS, VOS, which Stratus still supplies. However, application developers are generally more familiar with Unix. Many more applications run under Unix than under VOS, so the company now also offers FTX, its own version of Unix System V release 4 for multiprocessing (SVR4 MP). Sequoia and Tandem also offer OSs that run unmodified Unix applications. IMP and Themis use a standard OS—Sun Microsystems' Solaris, which is Unix-compatible.

Except for Solaris, these multitasking OSs incorporate hardened kernels, which are designed to prevent applications from causing system panics. (A "panic" is the Unix term for a crash.) The first objective is to contain each problem within the application in which it arose and not to let the problem affect other applications running concurrently. The system vendors have also rewritten key parts of Unix to prevent known problems. For example, Unix is known to panic when applications ask it to allocate more resources than a system can offer.

IMP adds fault tolerance to Solaris by using hardened device drivers. The company publishes the rules for writing these drivers so that peripheral-device suppliers can also write them. This approach is an important element of IMP's marketing strategy. The company markets its systems through telecommunications OEMs that incorporate the systems into products such as message switches and private branch exchanges (PBXs). Such systems include substantial amounts of specialized hardware, for which the communications OEMs must supply custom drivers.



You can obtain high-availability industrial PCs in configurations that mount in standard 19-in. racks, as this unit from Diversified Technology illustrates. A pair of redundant load-sharing ac or dc power supplies is at the left. Hot-swappable mirrored hard disks are at the right.

By now, you should understand that fault tolerance, whether provided by software on a network of standard workstations or by a combination of software and special hardware, offers benefits even in situations unrelated to faults. Upgrades to fault-tolerant systems' hardware and software need not cause service interruptions. You take the element to be upgraded off-line, perform the upgrade, and then put the element back on line.

However, when an upgrade involves stored information, you may have to wait quite awhile before the upgrade is really complete. When you load new software onto a mirrored drive, many hours or even days can pass before the image of the software on the counterpart disk becomes identical to that on the upgraded drive. The system must continue to function—albeit with degraded or nonexistent redundancy—while it synchronizes the drives' contents in the background. Depending on the quantity of data to be copied and the allowable degree of performance degradation, copying can take a substantial time.

Reference

1. Travis, Bill, "SCSI-based RAID systems provide storage redundancy, enhance data-transfer rate," *EDN*, Nov 23, 1994, pg 81.

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INDUSTRIAL ISSUE

Monolithic power amps provide diverse choices in circuit structures

BILL TRAVIS, SENIOR TECHNICAL EDITOR

When choosing a power-amplifier IC, take time to carefully consider the input and output characteristics that suit your application.

In the midst of the flurry of multimillion-transistor digital ICs assailing the marketplace, it's easy to forget that a wide variety of loads demands a lot of volts, amps, and watts to drive them. Some examples are motors, actuators, vibration-cancellation systems, and, of course, loudspeakers. The representative sampling of monolithic power amplifiers in **Table 1** can provide that needed drive. However, you must choose among them prudently to ensure that both the input and output characteristics satisfy the needs of your application.

Of the two sets of characteristics, those of the output stage are probably the more crucial to the success of your design. The worst that can happen if you choose an amplifier with inappropriate input parameters are inaccuracies accruing from offset and drift and, perhaps, undue loading of the source because of too-low input impedance.

Far graver woes can result from the choice of an amplifier whose output structure doesn't match the needs of the load. These woes include premature thermal shutdown and outright destruction of the amplifier IC. A discussion of the various output structures in **Fig 1** may offer some insight into the appropriateness of the various amplifier types for your application.

Figs 1a, **b**, and **c** are simplified output structures

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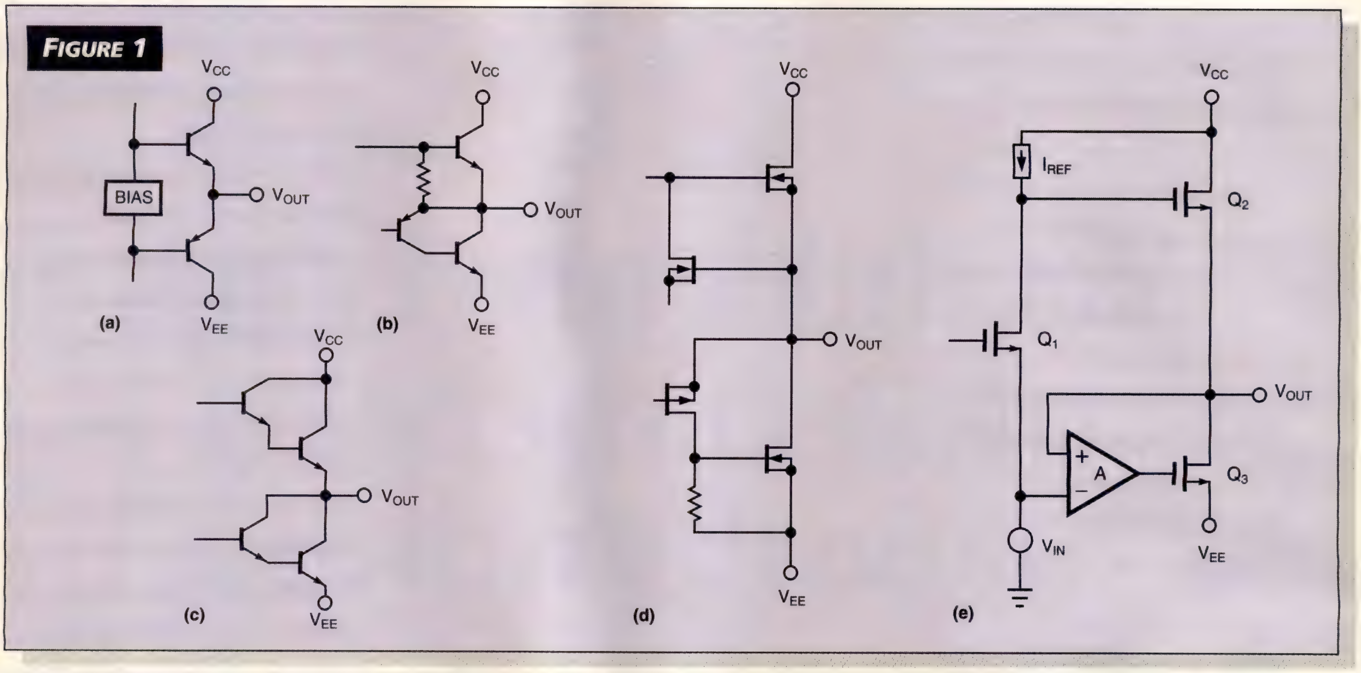
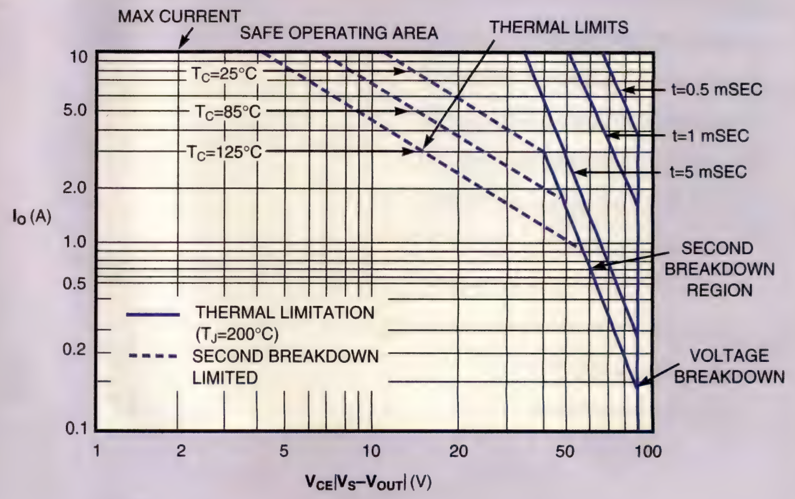
FIGURE 1



Bipolar output structures include full-complementary (a), quasi-complementary (b), and all-npn (c) types. The MOSFET structure in (d) suits high-voltage amplifiers; the structure in (e) suits low-distortion audio amplifiers.

FIGURE 2



When designing with bipolar amplifiers, you must be careful to keep the stress on the output transistors within the limits set by the safe-operating-area curves, especially in the solid-line region of second breakdown.

that use bipolar power transistors. You're not likely to find the full-complementary topology in **Fig 1a** in monolithic amplifiers, because high-power pnp transistors are not very amenable to monolithic processing. More's the pity, because, as **Ref 1** explains, the full-complementary stage is easy to use. It offers symmetrical output impedance and low crossover distortion (assuming proper class-AB biasing).

The quasi-complementary stage in **Fig 1b** is amenable to IC processing and provides performance similar to that of the full-complementary topology. The two lower transistors in the circuit form a "composite-pnp" transistor. The drawback to this structure is the heavy local feedback in the lower transistor loop, which can lead to instability in the presence of inductive loads.

The all-npn output stage in **Fig 1c** is an early approach to fabricating monolithic power amplifiers. Its main disadvantage is the large difference in output impedances when sourcing and sinking current. The upper (sourcing) transistor is an emitter follower with inherently low output impedance. The lower (sinking) transistor operates in common-emitter mode with inherently high output impedance. Another disadvantage is the large difference in open-loop gain in sourcing and sinking modes.

Beware of bipolar burnout

Bipolar power transistors are cursed with a negative temperature coefficient for V_{BE}, the base-emitter voltage required to yield a given collector cur-

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rent. So, unless a circuit designer incorporates compensation techniques into the output-stage drive circuitry, the power transistors are subject to thermal runaway. Power causes heating, heating causes V_{BE} reductions, and, with a given V_{BE} drive voltage, the transistor turns on even more fully. Without compensation precautions, this positive thermal feedback causes the transistor to self-destruct.

It's a tricky proposition to provide such V_{BE} compensation. A designer must strike a fine balance between two almost-conflicting criteria: maintaining adequate quiescent current to prevent crossover distortion and preventing thermal-runaway conditions.

An important consideration in matching bipolar output stages to the needs of a load is to respect the "safe operating area" (SOA) carefully. **Ref 2** gives a detailed explanation of how to use SOA curves for bipolar power transistors. **Fig 2** shows an SOA plot for a typical bipolar device. The maximum safe current is a function of V_{CE}.

At low values of V_{CE}, the transistor can deliver maximum current to the load. In this area of the SOA, the only worry is to avoid excessive currents that could overstress wire bonds or die metallization. As V_{CE} increases, the power dissipation increases to the point that self-heating raises the junction temperature to the maximum rated value (usually 200°C). Note that in this broken-line region, $V_{CE} \cdot I_C$ (power) is a constant.

As V_{CE} increases further, the safe output current decreases more rapidly. This area of the SOA plot is the *second breakdown* (also called secondary breakdown) region. Here, the transistor develops "hot spots" in regions of its

TABLE 1—REPRESENTATIVE INTEGRATED POWER AMPLIFIERS

Company	Model	Type	Output structure	Supply span (V)	Output current	Package	Price	Comments
Apex Microtechnology Circle No. 321	PA43	Monolithic MOSFET	n-channel MOSFET	350	120 mA peak	Surface-mount, dual-inline	$13.60 (10,000)	40-V/µsec slew rate; 2-mA quiescent current.
	PA45	Monolithic MOSFET	n-channel MOSFET	150	5A continuous	8-pin TO-3	$17.90 (10,000)	Uses BeO substrate for 1.5°C/W maximum junction-to-case resistance.
	SA01	PWM (Class D)	Full-bridge (push-pull) p- and n-channel MOSFETs	100	20A continuous	10-pin hermetic power package	$250 (100)	Switches at 45 kHz; drives 2-kW load. Contains error amp for motor control.
Burr-Brown Circle No. 322	OPA544	Monolithic FET-input	Bipolar	70	2A continuous	5-pin TO-220	$6.95 (100)	Combines FET op amp with bipolar power-output stage.
	OPA2544	Monolithic FET-input (dual OPA544)	Bipolar	70	2A continuous	8-pin TO-3	$22.25 (100)	Combines FET op amp with bipolar power-output stage.
National Semiconductor Circle No. 324	LM1876TF	Dual bipolar monolithic	Bipolar	54	2.9A (limit)	15-pin isolated TO-220 style	$3.20 (1000)	Protection circuit automatically monitors SOA conditions. Provides 2×15W to 4Ω or 8Ω loads.
	LM4700TF	Bipolar monolithic	Bipolar	64	2.9A (limit)	11-pin isolated TO-220 style	$2.50 (1000)	Protection circuit automatically monitors SOA conditions. Provides 25W continuous to 8Ω load.
SGS-Thomson Circle No. 325	TDA7294	Monolithic BiCMOS DMOS	DMOS	100	10A peak	15-pin plastic Multiwatt	$5.10 (10,000)	Delivers 100W music power, 70W rms. Contains mute/standby functions.
	TDA7295	Monolithic BiCMOS DMOS	DMOS	80	10A peak	15-pin plastic Multiwatt	$4.10 (10,000)	Delivers 80W music power, 56W rms. Contains mute/standby functions.
	TDA7296	Monolithic BiCMOS DMOS	DMOS	70	10A peak	15-pin plastic Multiwatt	$3.75 (10,000)	Delivers 60W music power, 42W rms. Contains mute/standby functions.

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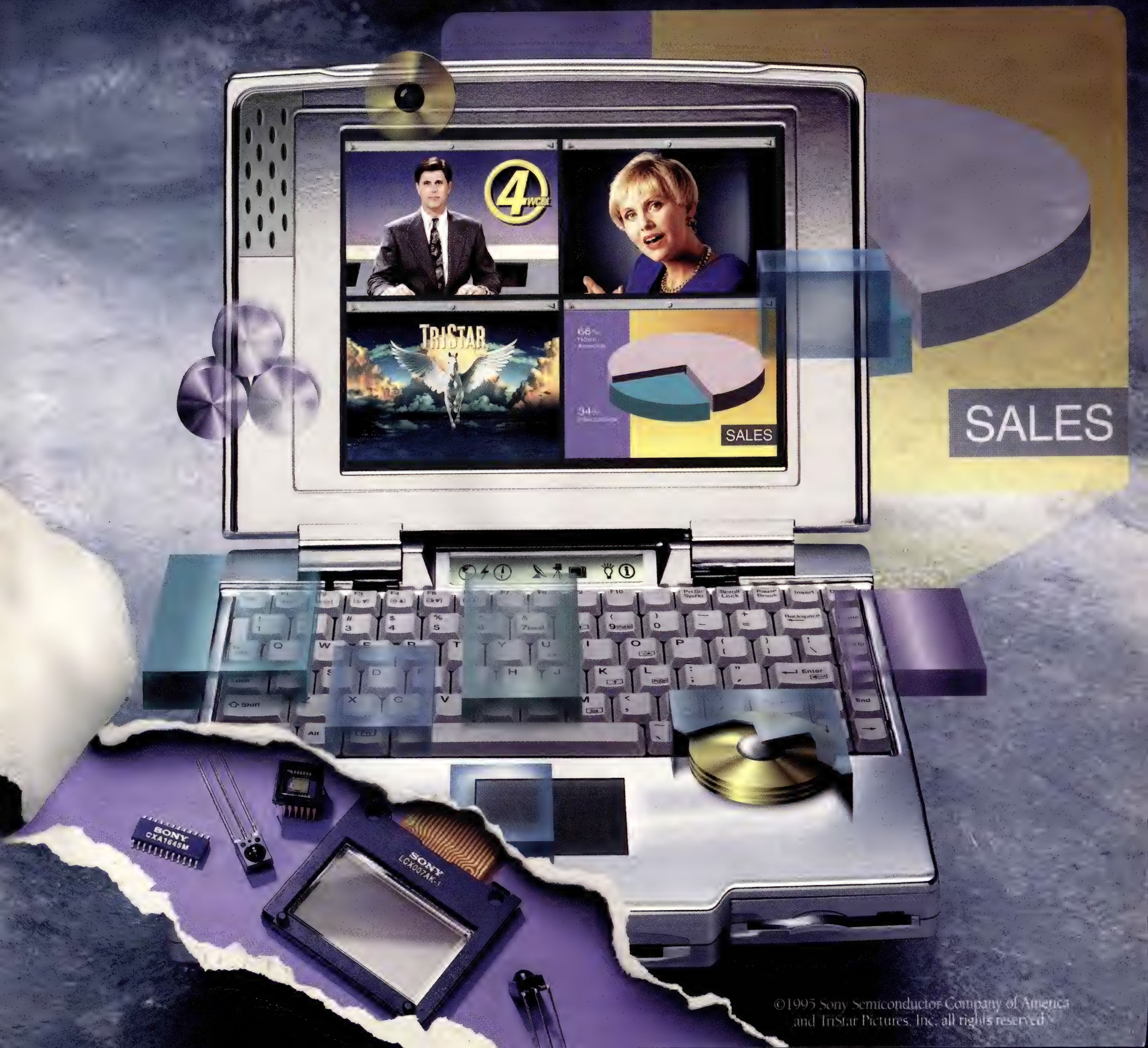

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geometry, points at which current flow concentrates. This condition leads to localized thermal runaway and, finally, device destruction. The final region of the SOA is the transistor's breakdown voltage.

Note the solid lines on the right side of the SOA plot in **Fig 2**. They indicate that you can exceed the second-breakdown limitations for short power pulses. Thanks to the thermal time constant of the silicon structure, such short-duration bursts of power don't give the transistor enough time to develop suicidal tendencies.

As **Ref 2** explains, you might be tempted to check for safe operation only at the point of maximum output voltage and current. But, this point may not be the most stressful. **Fig 3** is a plot of power dissipation as a function of the output voltage delivered to a resistive load. You can see that the worst-case dissipation for the amplifier occurs at 50% output voltage. You should use this condition to check for SOA compliance.

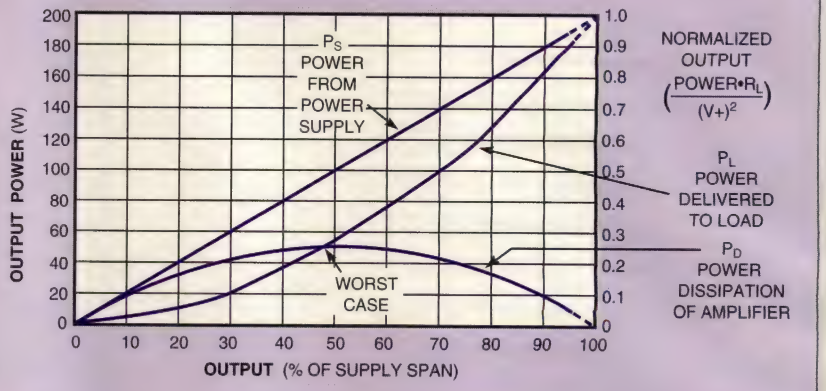
A short circuit to the negative rail is also a very stressful condition in the SOA. It forces the full power-supply voltage across the conducting transistor, and the current far exceeds the SOA limit. For this reason, amplifier designers incorporate thermal-shutdown circuitry in the ICs. For Burr-Brown's OPA544, for example, the short-circuit current is about 4A, and the safe SOA current is 1.5A. Thermal shutdown prevents device destruction.

Make note that the voltage in the horizontal axis of the SOA is not the amplifier's output voltage, but rather the voltage across the conducting transistor in the output stage. The vertical axis is the current delivered to the load. Also, be aware that capacitive or inductive loads can produce exceedingly stressful conditions in the output stage.

If a capacitive load is charged to the negative supply voltage and the output tries to go positive, the output instantaneously delivers maximum rated current at the full supply-voltage span. And, because an inductor acts as a current source, an analogous condition arises when the output tries to go negative.

National Semiconductor's bipolar-output parts (**Table 1**) incorporate a dynamic SOA-protection mechanism, called SPiKe, which stands for self-peak instantaneous Kelvin temperature-protection circuitry. National claims the circuitry makes the ICs nearly impervious to damage from instantaneous

FIGURE 3



Maximum amplifier power dissipation occurs not at the maximum output voltages, but rather at the midpoint of the output-voltage span. Make note of this fact when you check for SOA compliance.

TABLE 2—INTEGRATED-AMPLIFIER INPUT CHARACTERISTICS

Supplier	Model	Maximum offset (mV)	Maximum offset drift (µV/°C)	Maximum input-bias current	Input noise	Minimum common-mode rejection ratio (dB)
Apex Microtechnology **Circle No. 321**	PA43	30	130	200 pA	50 µV rms (typ) 10-kHz bandwidth 110 µV p-p (typ) 1 to 10 Hz	84
	PA45	10	50	100 pA	10 µV rms (typ) 10-kHz bandwidth	90
	SA0	10	No spec	5 µA	No spec	75
Burr-Brown **Circle No. 322**	OPA544/2544	5	10	100 pA	36 nV/√Hz (typ)	90
National Semiconductor **Circle No. 324**	LM4700/1876	15	No spec	0.5 µA	8 µV (max)	80
SGS-Thomson **Circle No. 325**	TDA7294/5/6	10	No spec	0.5 µA	5 µV (max) 20 Hz to 20 kHz	No spec

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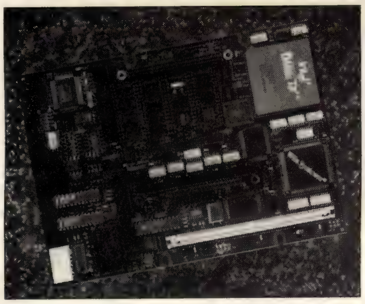

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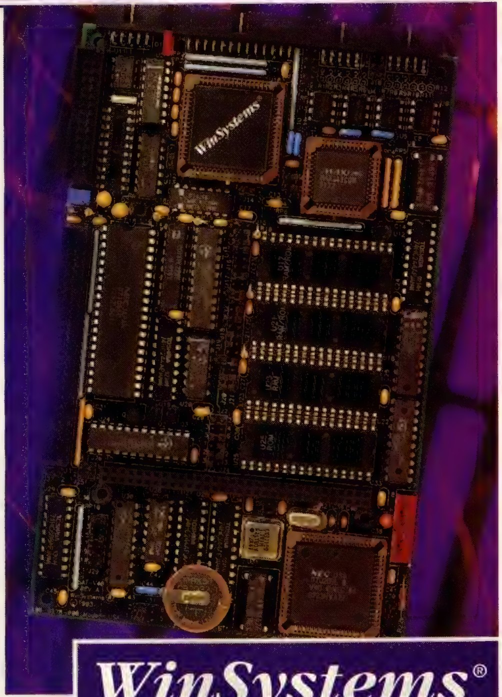

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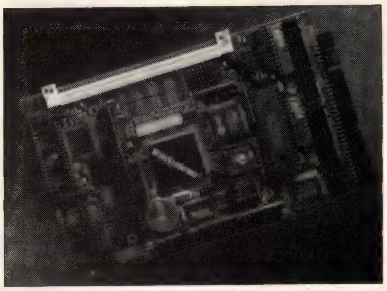

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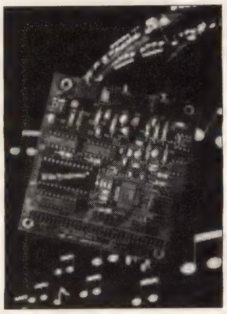

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temperature peaks and overvoltage and overcurrent conditions.

Banish second breakdown

Advances in IC processing make it possible to fabricate monolithic high-performance MOSFET amplifiers, a product line that was once the domain of multichip-hybrid manufacturers. Two advantages MOSFET amplifiers enjoy are low quiescent current and the absence of second-breakdown thermal runaway. The surface-mountable Apex PA43, for example, works with a total supply span of 350V and consumes only 2-mA quiescent current.

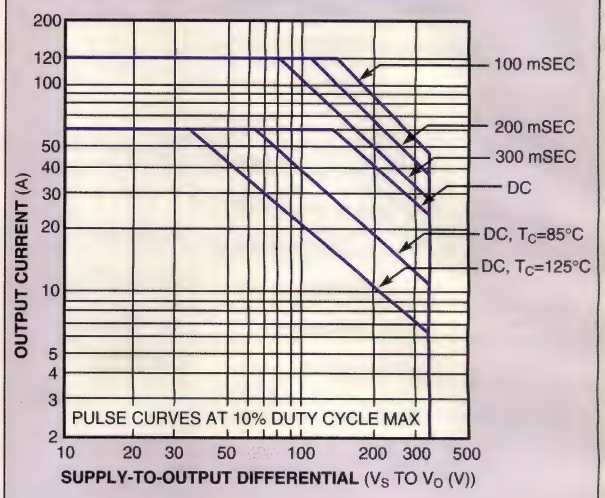
SOA considerations are not as crucial for MOSFET structures as they are for bipolar outputs. MOSFET output stages have two limitations: the current-handling capability of the die metallization and the temperature of the MOSFETs. For user convenience, Apex does publish SOA curves for its devices. **Fig 4** shows the SOA curves for the PA43, which has an output structure similar to that of **Fig 1d**. Note, again, that you can exceed SOA limits for short power pulses.

In **Table 1**, you can see that Apex's MOSFET amplifiers are high-voltage devices. High-voltage MOSFETs are much more amenable to IC processing than are bipolar transistors. These Apex amplifiers are general-purpose units, unlike the National and SGS-Thomson devices, which are characterized for audio applications. However, their application specificity doesn't prevent you from using them for other applications needing high-power drive.

The TDA729x Series from SGS-Thomson uses a mixed bipolar-CMOS-DMOS process to provide output-power levels from 60 to 100W to a loudspeaker. **Fig 1e** illustrates their output structure. SGS developed this novel architecture to ensure accurate control of quiescent current and to prevent crossover distortion. The quiescent current is a function of I_{REF} and the area ratio of Q_1 and Q_2, two adjacent DMOS transistors.

The local feedback afforded by the unity-gain block, A, in conjunction with the I_{REF}, Q_1 bias circuitry, prevents either transistor from cutting off completely. Complete cutoff would engender crossover distortion because of the relatively long recovery time of a cut-off MOSFET.

FIGURE 4



The SOA plot for Apex's PA43 MOSFET amplifier takes account of die-metallization current limits and output-MOSFET temperature. Note the absence of the second-breakdown region inherent in bipolar structures.

Like National, SGS employs a type of dynamic overload protection in the output stages of the TDA729x Series. Although the MOSFET output transistors are not subject to second breakdown, they are subject to destruction by overload. The protection circuitry senses the voltage and current—hence, power—in the output transistors and keeps the devices within SOA limits. It also uses a local temperature-sensing technique that dynamically controls the maximum dissipation.

Choose your input structure

In selecting a power-amplifier IC, you'll want to take a careful look at the devices' input characteristics. **Table 2** gives data-sheet parameters for the amplifiers listed in **Table 1**. Factors influencing your choice include source impedance, accuracy requirements, common-mode conditions, and noise performance.

The amplifiers from National Semi-

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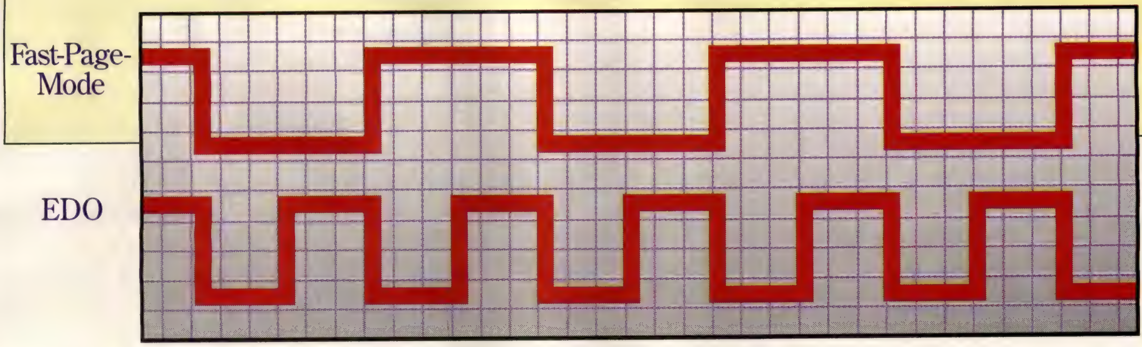

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	3.3V	60/70ns	25/30ns
512K x 32	5V	60/70ns	25/30ns
	3.3V	70ns	30ns
1M x 16	5V	60/70ns	25/30ns
	3.3V	70ns	30ns
4M x 4	5V	60/70ns	25/30ns
	3.3V	60/70ns	25/30ns
2M x 8	5V	60/70ns	25/30ns
	3.3V	60/70ns	25/30ns
1M x 18	5V	60/70ns	25/30ns
	3.3V	70ns	30ns

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LOOKING AHEAD

Considering the power-amplifier ICs in this article, two trends begin to crystallize. First is the demise of multichip-hybrid amplifiers in the wake of the onslaught of high-performance monolithic devices. Gone are the halcyon days of such hybrid-amplifier makers as the late, lamented Teledyne Philbrick. After all, who wants to pay $200 for a hybrid amplifier when you can get a monolithic device with equivalent or better performance for $10?

The hybrids had their day because of the severe constraints monolithic ICs placed on analog-circuit designers. Back in the '80s, circuit-design wizards, such as the late Bob Widlar, learned how to live with, and even exploit, these former constraints. Widlar designed, for example, National Semiconductor's PA12, whose clever circuit topology made intelligent use of monolithic structures to provide thermal protection, emitter ballasting, and other useful bells and whistles. To put it succinctly, there is practically nothing an expensive hybrid can do that an inexpensive monolithic can't do.

The second trend centers around advances in processing technology, advances that made the amplifiers discussed in these pages possible. These advances will engender more and better power amplifiers in the future. A couple of examples are Burr-Brown's combining FET-input amplifiers with bipolar output stages and SGS-Thomson's use of a bipolar-CMOS-DMOS amalgam. These mixed-technology processes make it possible to enjoy the best of all worlds (depending on your application) in parameters such as input impedance, offset, and drift, as well as power consumption, output robustness, and available swing.

One final prediction: Bet on the emergence of more PWM-amplifier ICs like Apex's SA01; also, expect these types, too, to "go monolithic" as IC processing progresses. In this world of ever-increasing power frugality, the technical allure and marketing appeal of >90% efficiency is too great to resist.

conductor and SGS-Thomson use bipolar input stages. This fact is evident from the relatively high, 0.5-μA maximum input-bias currents. Therefore, you'd probably not select these types for applications having extremely high driving-source impedances. In **Table 2**, note that these amplifiers offer no offset-drift specs. As stated, they're designed principally as audio amplifiers, so drift is of relatively limited importance.

In judging whether the noise performance of an amplifier suits your application, you'll have to do some translation between the different style specs of the various amplifiers. For example, Burr-Brown's OPA544 specs 36 nV/√Hz typical, and the other amplifiers spec either wideband or limited-band rms or p-p voltage figures.

Maximum offset voltages range from the OPA544's 5 mV to the PA43's 30 mV. If the 30 mV seems high, remember that the PA43 is a 350V amplifier intended for applications such as telephone-ring generators, piezoelectric positioning, and electrostatic transducers and deflection circuits—applications in which offset is of little importance.

Monolithic amplifiers go digital

Just when we thought the amplifier-IC world was safe from the "fully on, fully off" mentality of digital technology, along comes Apex Microtechnology's SA01, a high-power device that occupies only 2 in.^{2} and delivers 2 kW to its load (**Ref 3**). This hybrid amplifier uses pulse-width modulation (PWM), or Class-D operation, to provide power amplification.

This device is a breakthrough in that such power levels were formerly available only from large "bricks" and chassis-mounted PWM amplifiers. The SA01 provides a full H-bridge (push-pull) output, effectively doubling the power available from a given single power supply.

Although this device's operating principle is not strictly "Boolean," you can consider it a digital circuit in the sense that its output stage only switches fully on and off and spends no time (except during transitions) in the linear region. The result is >90% efficiency, as opposed to the wasteful 50% inherent in linear amplifiers. The device is useful in applications such as brush-type motor control, magnetic coils for MRI systems, and vibration cancellation.

If the idea of rolling your own switching amplifiers appeals to you, read Jeff Sherman's *EDN* article (**Ref 4**), which shows how to use Harris Semiconductor's MOSFET-driver ICs to configure highly efficient, low-distortion amplifiers.

You now have available a variety of monolithic power amplifiers to fit almost any conceivable application. In selecting one, take care to match the input and output characteristics and limitations to the needs of your system. EDN

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4. Sherman, Jeffrey, "Class D amplifiers provide high efficiency for audio systems," *EDN*, May 25, 1995, pg 103.

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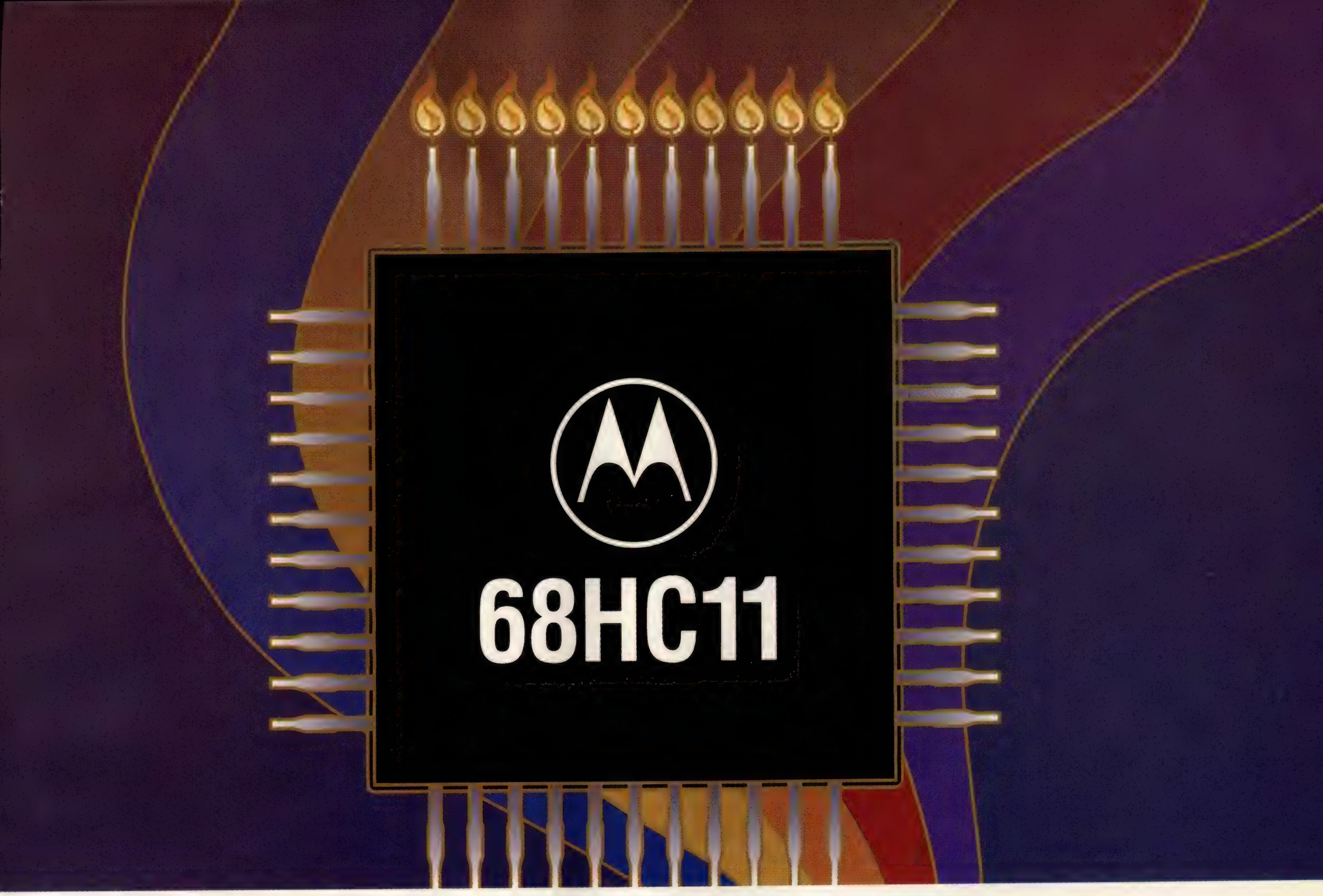

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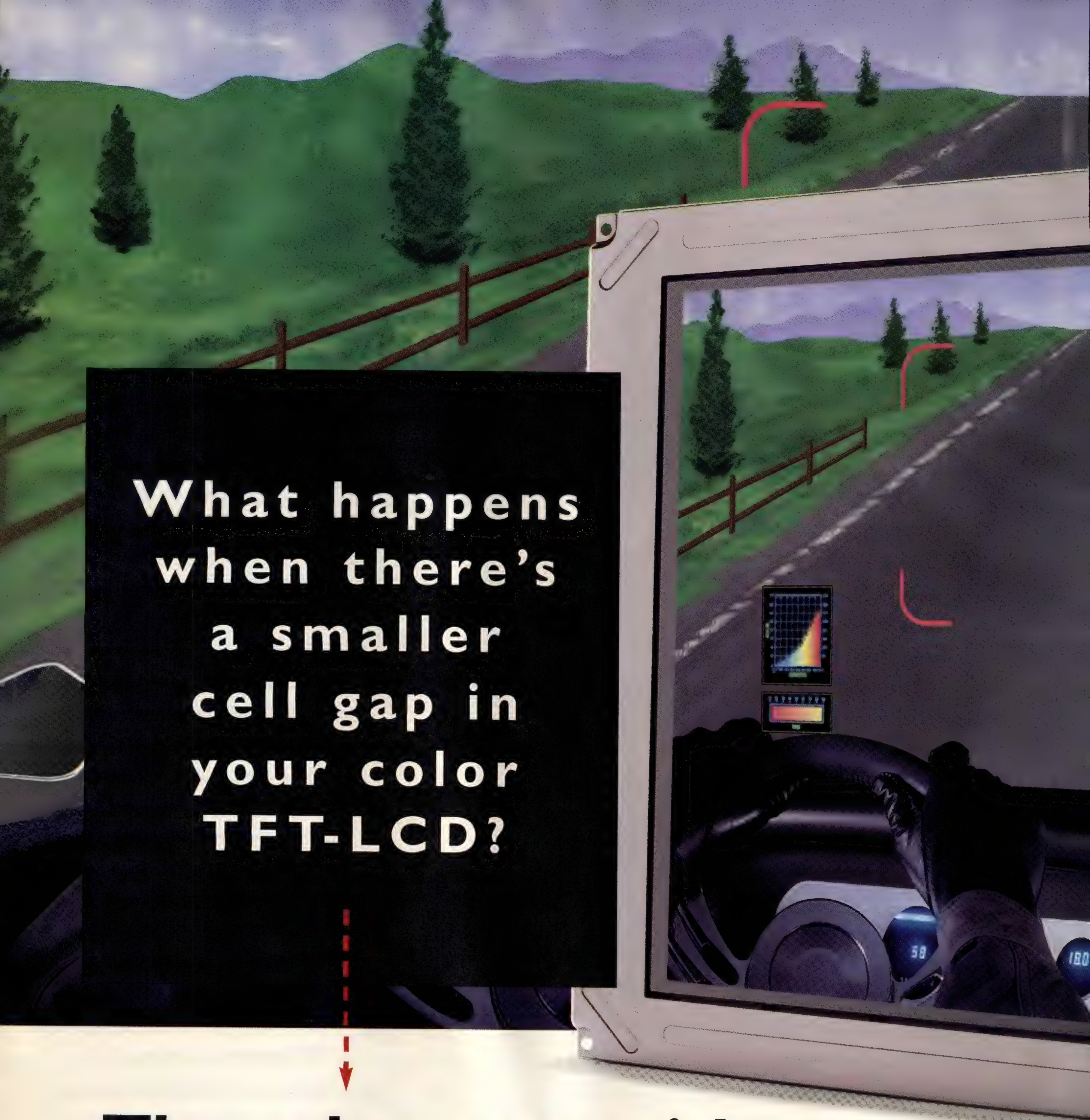

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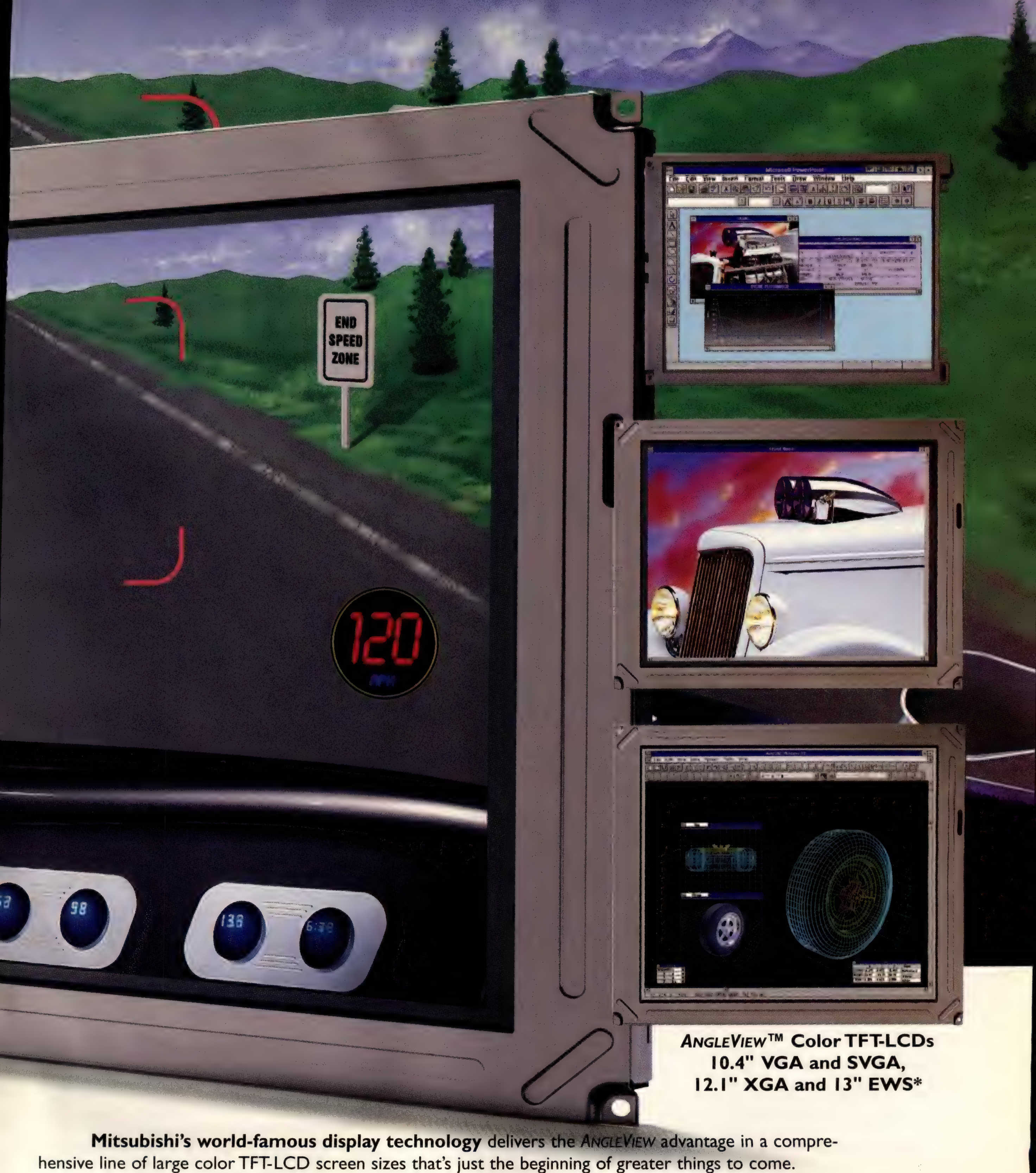

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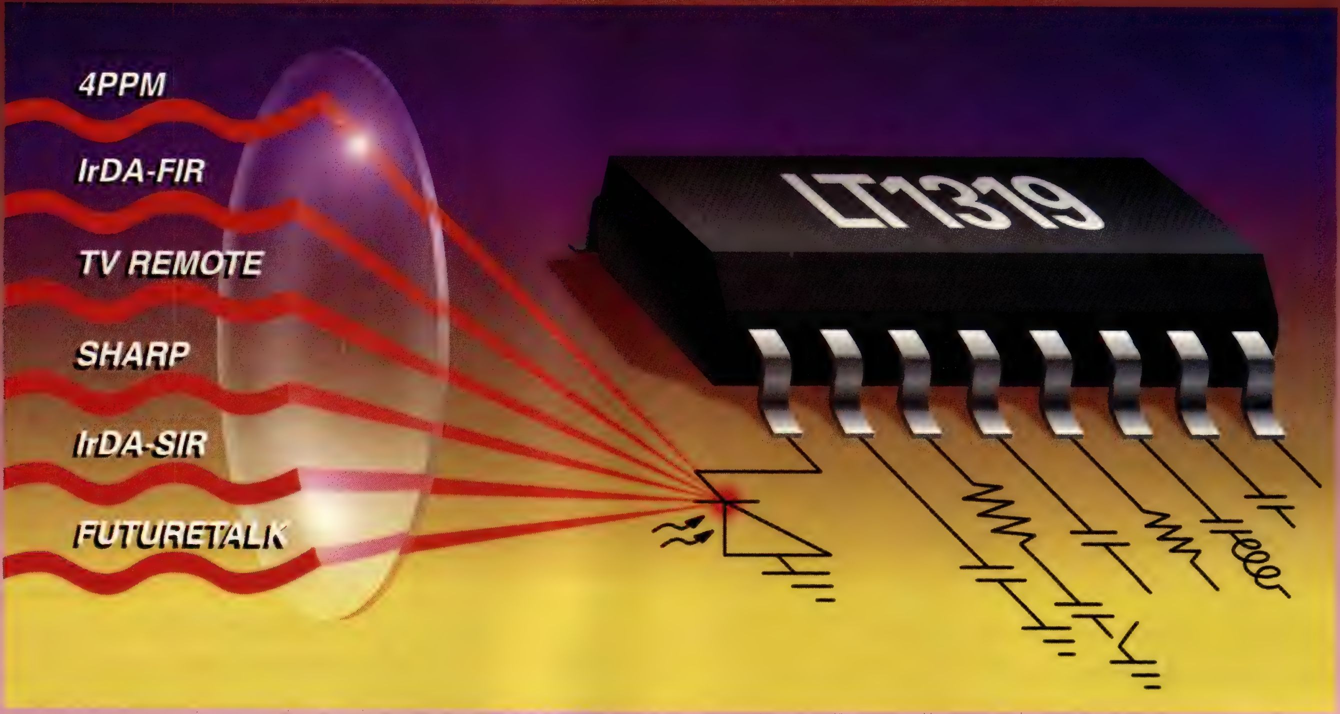

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Raphael Horton is always glad to get complaints. "It means designers are actually using my circuit," says Horton, an applications engineering projects manager for Exar Corp in San Jose, CA. Horton is the 1994 *EDN* Design Ideas grand-prize winner. As Horton gleefully accepts his $1500 prize, he admits to having received lots of complaints (as well as compliments) about his winning circuit, "Color video travels on twisted-pair cable," which appeared in *EDN* Design Ideas on February 3, 1994 and is reprinted on the next page. Horton says that designers often call to complain that they cannot obtain the same performance from their current wire gauge, or because they want to debate transmission-line theory with him. But, Horton is always glad to listen. "I've often thought about changing my title to applications-engineering psychotherapist," he quips.

Horton's winning circuit design allows video-system designers to use inexpensive twisted-wire cables, such as those in telephone lines and LANs, to transmit composite-color-video signals anywhere phone lines exist. His idea is practical, and it saves time and money. If an application requires just 500 ft of cable, for example, the cost difference could exceed $65, which more than justifies the added cost of a few LM6181 amps in his circuit.

Design Ideas Editor Bill Travis attributes the appeal of Horton's Design Idea to its universal usefulness. Travis says that it belongs to that class of innovative ideas that inspires readers to smack themselves on the head and say, "Wow, that's clever! Why didn't I think of that?"

Raphael Horton is currently working as an application engineering projects manager for Exar Corp's data-acquisition-products group in San Jose, CA. He has developed several hardware, firmware, and software systems, working with CCD-based video, imaging, and scanning applications. To forward complaints (or congratulations), you can reach Horton by phone at (408) 434-6400, ext 3408.—by Jim Leonard

Each issue, *EDN* readers vote for their favorite Design Idea. Winners receive $100 and automatically qualify for the annual grand-prize contest. The following list contains all of the 1994 winners. Congratulations to all of our Design Ideas contributors—and keep the innovative ideas coming.

January 6, 1994: "Classic detector enables low-cost receiver," Charles Kitchin, Analog Devices Inc (Wilmington, MA).

January 20, 1994: "PC programs PROM simulator," Shwang-Shi Bai, Chang-Shan Institute of Technology (Taiwan, ROC).

February 3, 1994: "Color video travels on twisted-pair cable," Raphael Horton, National Semiconductor (Santa Clara, CA).

February 17, 1994: "Off-line power supply requires few parts," Sam Ochi, IXYS Corp (Santa Clara, CA).

March 3, 1994: "Pressure gauge responds linearly to altitude," Bruce Trump, Burr-Brown Corp (Tucson, AZ).

March 17, 1994: "Digital potentiometer controls LCD bias," Michael Cortopassi, Dauphin Technology (Lombard, IL).

March 31, 1994: "Low-cost converter drives fluorescent tubes," Steven Hageman, Calex Manufacturing Co (Concord, CA).

April 14, 1994: "Technique targets board parasites," Rea Schmid, Comlinear Corp (Ft Collins, CO).

April 28, 1994: "3½-digit DVM IC measures power factor," Devadoss John and KRS Sarma, Hindustan Cables Ltd (Hyderabad, India).

May 12, 1994: "Laser printer prototypes pc-board artwork," Raj Shah and Dan Meeks, Q-bit Corp (Palm Bay, FL).

May 26, 1994: "Simple module gives voice to PC," Jerzy Chrzaszcz, Institute of Computer Science, Warsaw University of Technology (Warsaw, Poland).

June 9, 1994: "Printer-port data appears as bar on PC screen," Yongping Xia, EBT Inc (Torrance, CA).

June 23, 1994: "Dual microphones separate voice from noise," Samuel Kerem, Infrared Fiber Systems (Silver Spring, MD).

July 7, 1994: "10-octave audio generator speeds tests," Wayne Sward, Consultant (Bountiful, UT).

July 21, 1994: "Negatrons enrich filter, oscillator designs," Aleksandr Belousov (Baltimore, MD).

August 4, 1994: "RC network eliminates precision reference," Christophe Basso, European Synchrotron Radiation Facility (Grenoble, France).

August 18, 1994: "$10 receiver has microvolt sensitivity," Charles Kitchin, Analog Devices Inc (Wilmington, MA).

September 1, 1994: "Solid-state relay saves battery's life," Tom Gay, Siemens (Regensburg, Germany).

September 15, 1994: "Switch conserves microcontroller's I/O pins," Franklyn Dahlberg Jr, US Air Force (Hill AFB, UT).

September 29, 1994: "PC acts as RS-232C protocol analyzer," JS Holmes, Boehringer Mannheim (Indianapolis, IN).

October 13, 1994: "Serial-controlled 'postage stamp' computer governs process," Steven Hageman, Calex Manufacturing Inc (Concord, CA).

October 27, 1994: "Peltier element controls itself," Dmitrii Loukianov, Intel Corp (Moscow, Russia).

November 10, 1994: "Oscillator keeps THD below 1 ppm," Jeff Smith, Analog Devices Inc (Wilmington, MA).

November 23, 1994: "IC adds full-duplex RS-485 operation," Ron Clark, Maxim Integrated Products (Sunnyvale, CA).

December 8, 1994: "Battery-powered sensor detects dangerous UV radiation," Joerg Hollman, Hughes Leitz (Ontario, Canada).

December 22, 1994: "Pseudonoise generator doubles its speed," RN Mutagi, Space Applications Centre (Ahmedabad, India).

1994
GRAND PRIZE
WINNER

Color video travels on twisted-pair cable

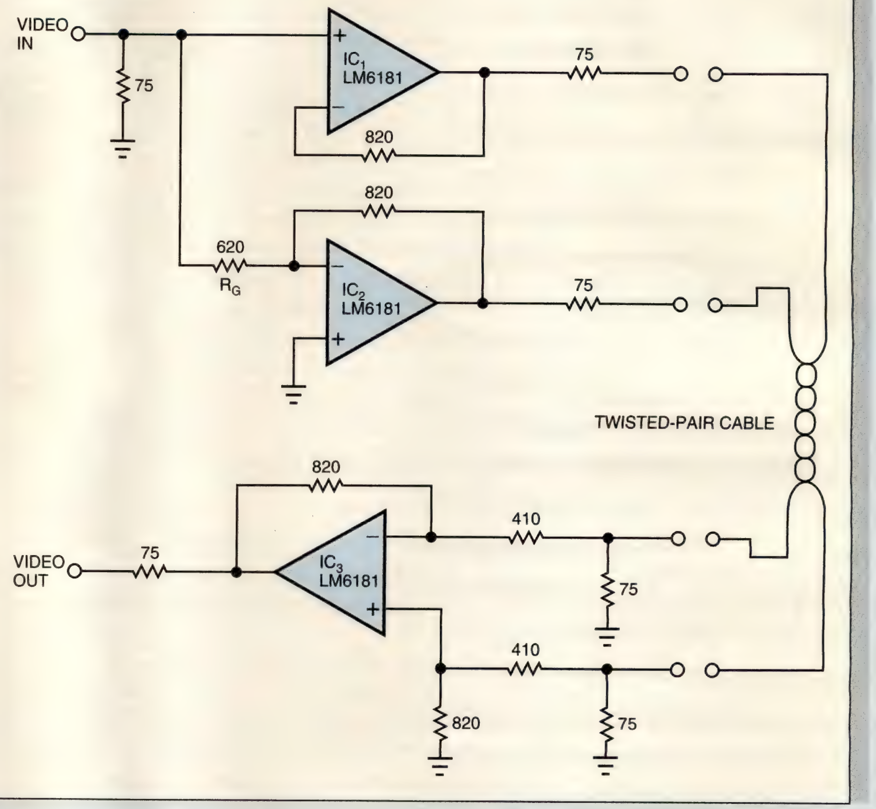
RAPHAEL HORTON, NATIONAL SEMICONDUCTOR, SANTA CLARA, CA

Telephone lines and local-area networks commonly use inexpensive twisted-pair cables. Video-system designers can also take advantage of this low-cost cable to transmit composite-color-video signals. Using the circuit techniques in **Fig 1**, you can transmit video anywhere phone lines exist. Although the circuit has more electronic components than the traditional single amplifier used to drive a coax cable, you can easily justify the additional electronics required to drive twisted-pair cables. Four-wire, twisted-pair cable typically sells for 7 cents/ft, yet RG-59 cable can be priced over 20 cents/ft. If just 500 ft of cable is necessary, the cost difference is $65, which more than covers the cost of a few LM6181 amplifiers.

The system consists of two circuits. The first converts the composite video signal to a differential signal using amplifiers IC$_1$ and IC$_2$. Using a differential signal reduces line loss and distortion that could occur from driving the twisted pair single ended. Converting the signal to differential also removes possible ground-plane errors that occur when there is a difference in the ground potential between two pc boards.

The circuit has a minimum signal gain of two to compensate for the terminations' 6-dB signal drop. You can easily adjust the gain of IC$_2$ by decreasing the value of R$_G$ to make up for the line losses caused by various twisted-pair and coax cable lengths. R$_G$ serves as a single system adjust and as an optional contrast adjustment for the video system.

FIGURE 1



By transmitting differential signals and using video amplifiers with high-output-drive capability, this circuit can drive video signals down inexpensive twisted-pair cable.

In the second circuit, IC$_3$ converts the differential signal back to single ended. This circuit has a gain of two to drive a back-terminated RG-59 coax cable out to a monitor. The video amplifier you choose for this application must have high-output-drive capability. The LM6181 is guaranteed to drive a back-terminated 75Ω cable over the full industrial temperature range.

This circuit treats the twisted-pair cable as a transmission line that is back-terminated with 75Ω resistors. This termination method is superior to using the 600Ω characteristic impedance of the twisted-pair. A 600Ω termination results in smearing and blurring caused by the RC time constant of the cable capacitance and the termination resistance. Because an increasing RC time constant degrades sharp signal transitions, this circuit uses standard 75Ω terminations to maintain a clear, sharp picture. This circuit does not use shielded twisted-pair cable because of its high distributed capacitance, which contributes to the RC time constant.

No visible difference exists between a reference picture and a transmitted one. Using a Tektronix-type 520 NTSC vector-scope, the measured differential gain and phase of the entire system—which comprises three LM6181 amplifiers, a 100m twisted-pair cable, and a 50-ft RG-49 coax cable from amplifier IC$_3$—was less than 0.5% and 0.6°, respectively. Keeping the current-feedback amplifiers' feedback resistors equal to the recommended value of 820Ω gives the op amp its proper frequency compensation. The feedback resistor sets amplifier bandwidth and is always required for proper operation, even in unity gain. **EDN BBS /DI_SIG #1361**

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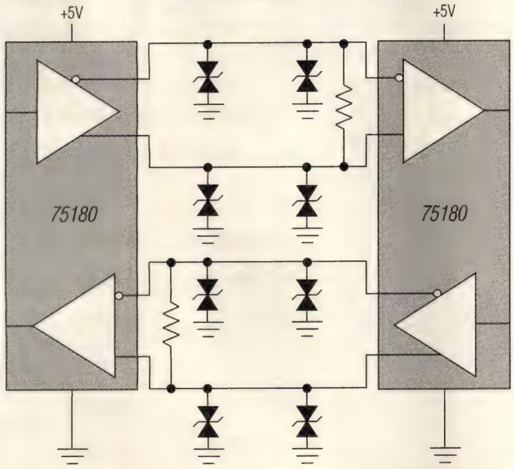

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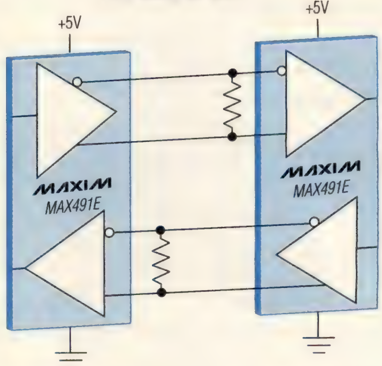

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MAX483E	1/1	±15kV	Yes	0.25	Half	32	75176	1.50
MAX485E	1/1	±15kV	Yes	2.5	Half	32	75176	1.50
MAX487E	1/1	±15kV	Yes	0.25	Half	128	75716	1.50
MAX488E	1/1	±15kV	Yes	0.25	Full	32	75179	1.50
MAX489E	1/1	±15kV	Yes	0.25	Full	32	75180	1.50
MAX490E	1/1	±15kV	Yes	2.5	Full	32	75179	1.50
MAX491E	1/1	±15kV	Yes	2.5	Full	32	75180	1.50
MAX1487E	1/1	±15kV	Yes	2.5	Half	128	75176	1.50

*MAX491E is available now. Contact the factory for availability of all other parts.
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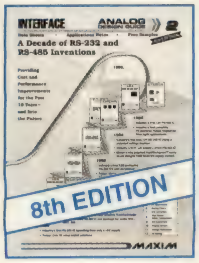

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CIRCLE NO. 44

Voltage controls sine-wave frequency

YONGPING XIA, EBT INC, TORRANCE, CA

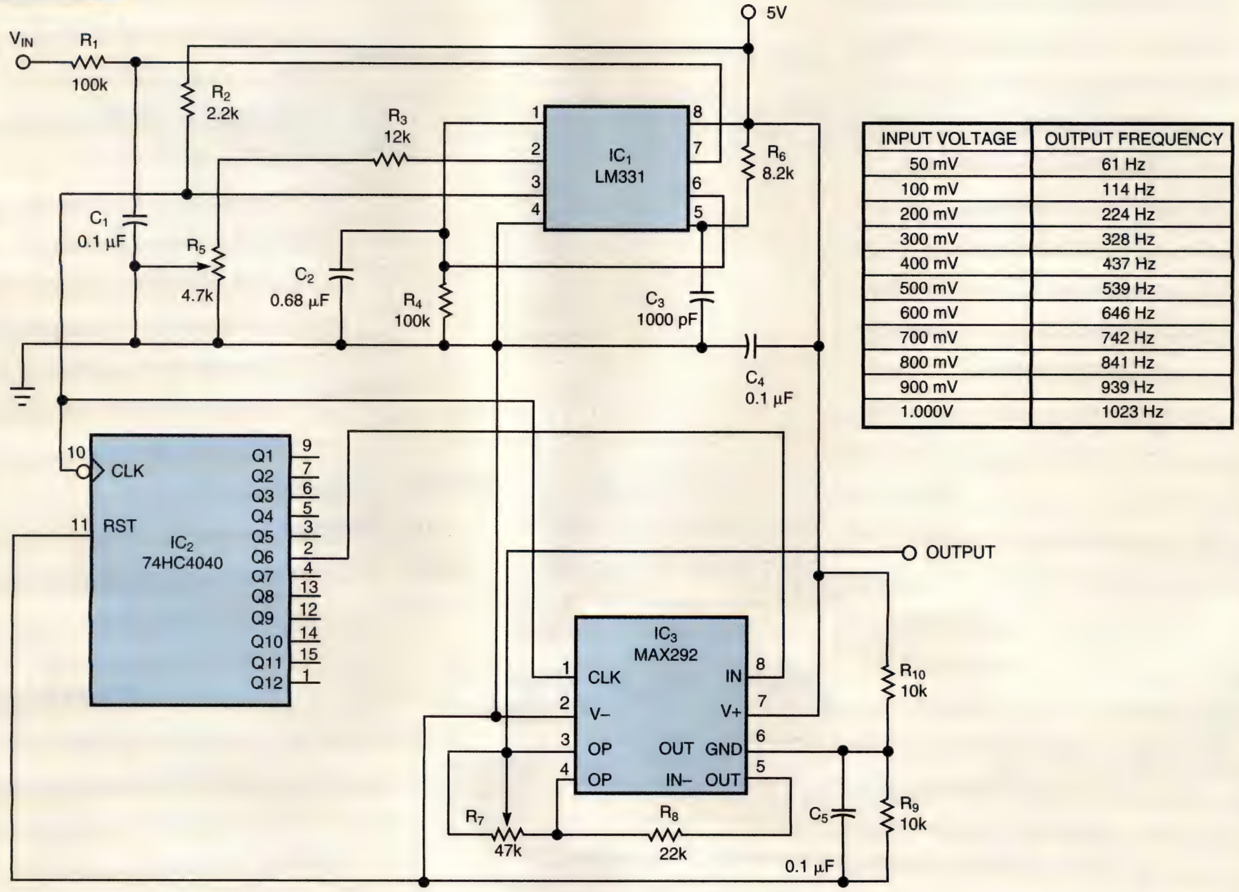
The circuit in **Fig 1** generates a 50-Hz to 1-kHz sinusoidal waveform that exhibits lower than –60-dB THD. The input voltage controls the output frequency with the relationship 1 kHz/V. The output amplitude is invariant with frequency over the entire operating range. IC_1 is a V/F converter with an input control range of 0 to 1V. You adjust R_5 so that the output frequency equals 1 kHz with a 1V input.

IC_3 is a switched-capacitor lowpass filter. The clock frequency, provided by IC_1, determines the filter's –3-dB corner frequency in the ratio of 100:1. Thus, the corner frequency is 100 Hz if IC_3's clock frequency is 10 kHz. Meanwhile, IC_2 divides the clock frequency by 64 to provide the input to IC_3. Because the input frequency is higher than 1/100th of the clock frequency, only the fundamental of the square-wave input can partially pass through the filter. The fundamental passes through the filter with about an 8-dB loss. The total harmonic content is lower than –60 dB.

A built-in operational amplifier amplifies the filter's output. You can adjust R_7 to change the output amplitude. Because the ratio of IC_3's input and the clock frequency is always a constant, the output amplitude remains constant throughout the entire operating-frequency range. (DI #1745) EDN

To Vote For This Design, Circle No. 388

FIGURE 1


5V
V_{IN}
R_1
100k
R_2
2.2k
R_3
12k
1
2
3
4
8
7
6
5
IC_1
LM331
R_6
8.2k
C_1
0.1 μF
R_5
4.7k
C_2
0.68 μF
R_4
100k
C_3
1000 pF
C_4
0.1 μF
10
CLK
11
RST
IC_2
74HC4040
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
9
7
6
5
3
2
4
13
12
14
15
1
OUTPUT
IC_3
MAX292
CLK
V–
OP
OP
IN
V+
OUT GND
IN– OUT
R_7
47k
R_8
22k
C_5
0.1 μF
R_{10}
10k
R_9
10k

INPUT VOLTAGE	OUTPUT FREQUENCY
50 mV	61 Hz
100 mV	114 Hz
200 mV	224 Hz
300 mV	328 Hz
400 mV	437 Hz
500 mV	539 Hz
600 mV	646 Hz
700 mV	742 Hz
800 mV	841 Hz
900 mV	939 Hz
1.000V	1023 Hz

Low harmonic distortion and a 100:1 tuning range are the salient features of this voltage-controlled sine-wave generator.

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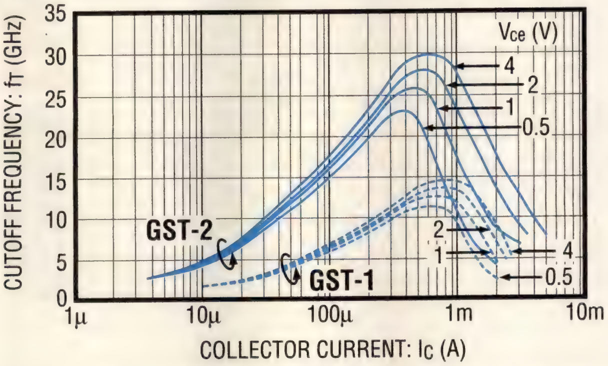
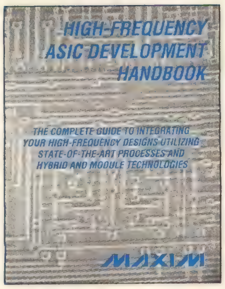


Our GST-2 process can reduce power consumption significantly in wireless and RF systems. Cutoff frequencies of 10GHz are possible with collector currents as low as 30µA.



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- **Dual Lowpass Active Filters**
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- **Power-Amp Driver**
- **Quadrature Modulator**
- **900MHz Upconverter**
- **IF Amplifier**
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CIRCLE NO. 45

Precharged capacitor ensures high-side start-up

CHRISTOPHE BASSO, EUROPEAN SYNCHROTRON RADIATION FACILITY, GRENOBLE, FRANCE

When you use a high-voltage bridge driver, such as the IR2110 or the newer IR2155, a complete driver circuit can exhibit erratic behavior when you apply power. The main problem arises from the bootstrap capacitor that discharges when the power appears. Thus, the floating supply is not ready to fulfill its primary function of driving the high-side MOSFET. The circuit needs a few commutations to rapidly charge the bootstrap capacitor to allow it to supply the upper driver.

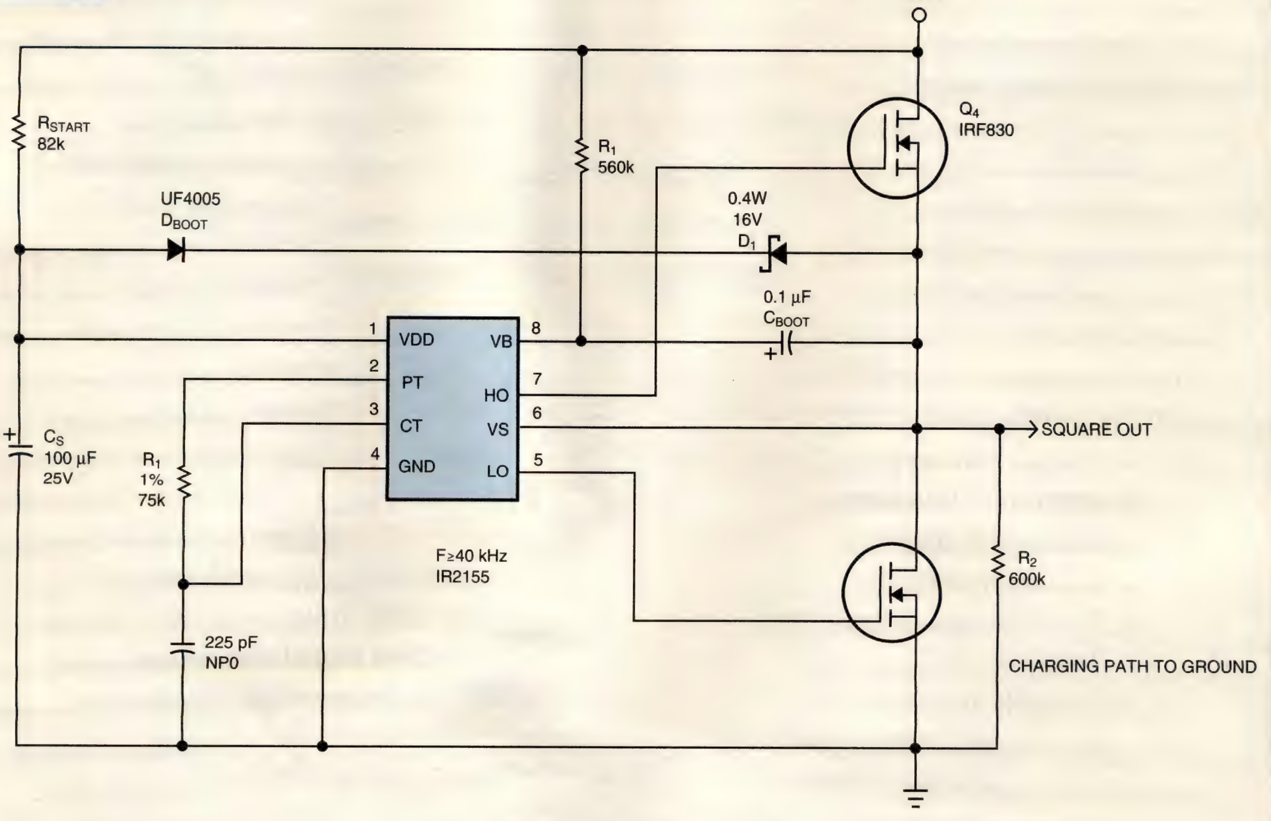
Unfortunately, this short period of unstable power conditions produces erratic driver behavior. For example, in fluorescent ballasts, in which a frequency sweep implements a preheat operation, the erratic start-up behavior creates a brief illumination in the tube. This illumination diminishes the benefits of a hot-cathode start. The simple configuration in **Fig 1**, which joins a high-voltage resistor and a 400-mW, 16V zener diode, cures the problem of erratic start-up.

The main supply directly feeds the IR2155. However, you can extend the method to other topologies, such as a ballast supplied by a power-factor-corrected auxiliary supply. At power-up, R_1 precharges C_{BOOT} via the R_2 resistive path to ground. Zener diode D_1 limits the voltage across C_{BOOT} to 16V. This limiting action protects the upper driver from damage by overvoltage. Thus, when the IR2155's V_{CC} pin reaches the upper threshold level, C_{BOOT} is already charged and the MOSFET bridge delivers square waves without exhibiting erratic behavior.

The fluorescent tube's cathode, thus, receives a proper preheat before the complete strike occurs. Your only caveat is to ensure that the $R_1 \cdot C_{BOOT}$ time constant is lower than the RC time constant of the IR2155's power-supply network. (DI #1747) EDN

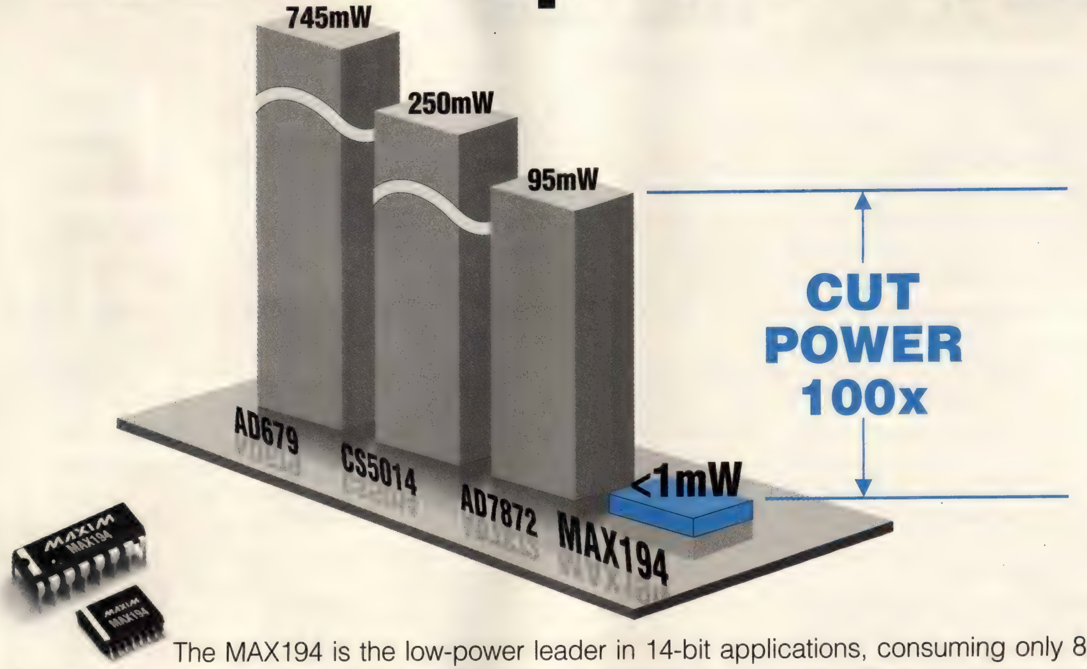
To Vote For This Design, Circle No. 389

FIGURE 1



Precharging the bootstrap capacitor in a high-side MOSFET-driver circuit eliminates erratic behavior during start-up.

LOWEST POWER, 85ksps 14-BIT ADC HAS 10µA SHUTDOWN



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CIRCLE NO. 46

Circuit drives 9V solenoids from 3V battery

CRAIG VARGA, LINEAR TECHNOLOGY CORP, MILPITAS, CA

At times, it may be necessary to power a solenoid-type pulsed actuator from a low-voltage battery in portable equipment. The circuit in **Fig 1** accomplishes this task using a standby current of 10 μA. The design takes advantage of the fact that solenoids like being actuated by capacitive discharge at much higher levels than their nominal voltage. This mode of operation results in a good, crisp response by the solenoid plunger.

IC_1 is a micropower boost converter powered directly from a 3V lithium battery. As long as the ACTUATE line is low, IC_1 is in standby mode and consumes little current. When ACTUATE goes high, IC_1's pin 3 goes low. C_1 couples this low-going edge into the feedback divider comprising R_1, R_2, and R_3, which pulls the LBI pin of IC_1 below the IC's internal reference. LBO then goes low, tying the bottom of the feedback divider to ground.

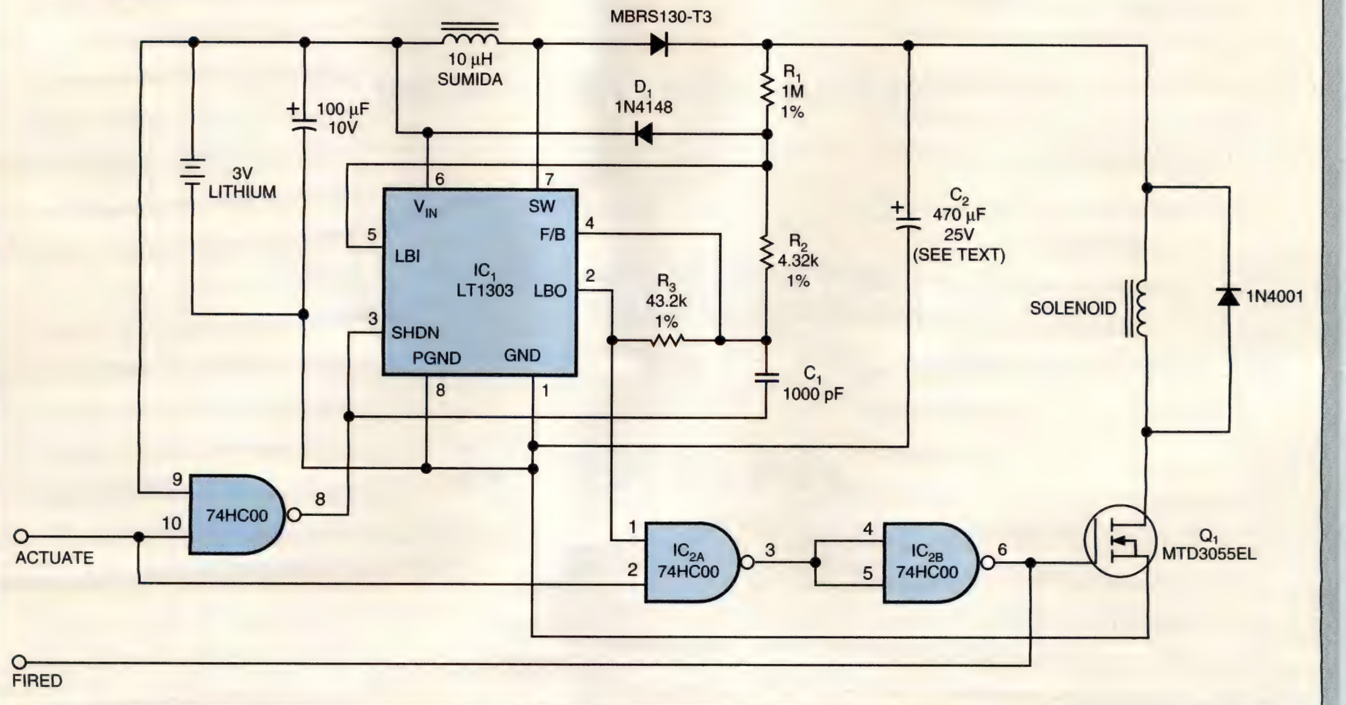
IC_1 then begins to switch at approximately 150 kHz, gradually charging C_2. When C_2's voltage reaches 21V (which takes approximately 0.15 sec), the voltage at LBI crosses the 1.24V reference threshold, forcing LBO's open-collector output high. IC_{2A} and IC_{2B} buffer this signal and drive MOSFET Q_1's gate high, allowing the energy stored in C_2 to dump into the solenoid coil. Because LBO is now high, the voltage at LBI is also high and stays that way. Thus, the FET stays energized until nearly all of C_2's energy dumps into the solenoid.

The FIRED signal reports to the system that the solenoid has fired and that the circuit should now be disabled. D_1 clamps the feedback to V_{IN}. The feedback divider sets the voltage limit on C_2 to about 23V. This setting ensures that overvoltage won't destroy IC_1's internal power switch should the solenoid coil open or become disconnected.

The size of C_2, which you choose empirically, depends on the particular solenoid. To choose C_2, charge up larger and larger capacitors to approximately 18V, and connect the solenoid to the charged capacitor until you find a size that reliably fires the solenoid. Using the next larger capacitor and 21V to fire the solenoid provides some design margin. (DI #1741) EDN

To Vote For This Design, Circle No. 390

FIGURE 1



This solenoid driver operates off a 3V battery and requires a standby current of just 10 μA.

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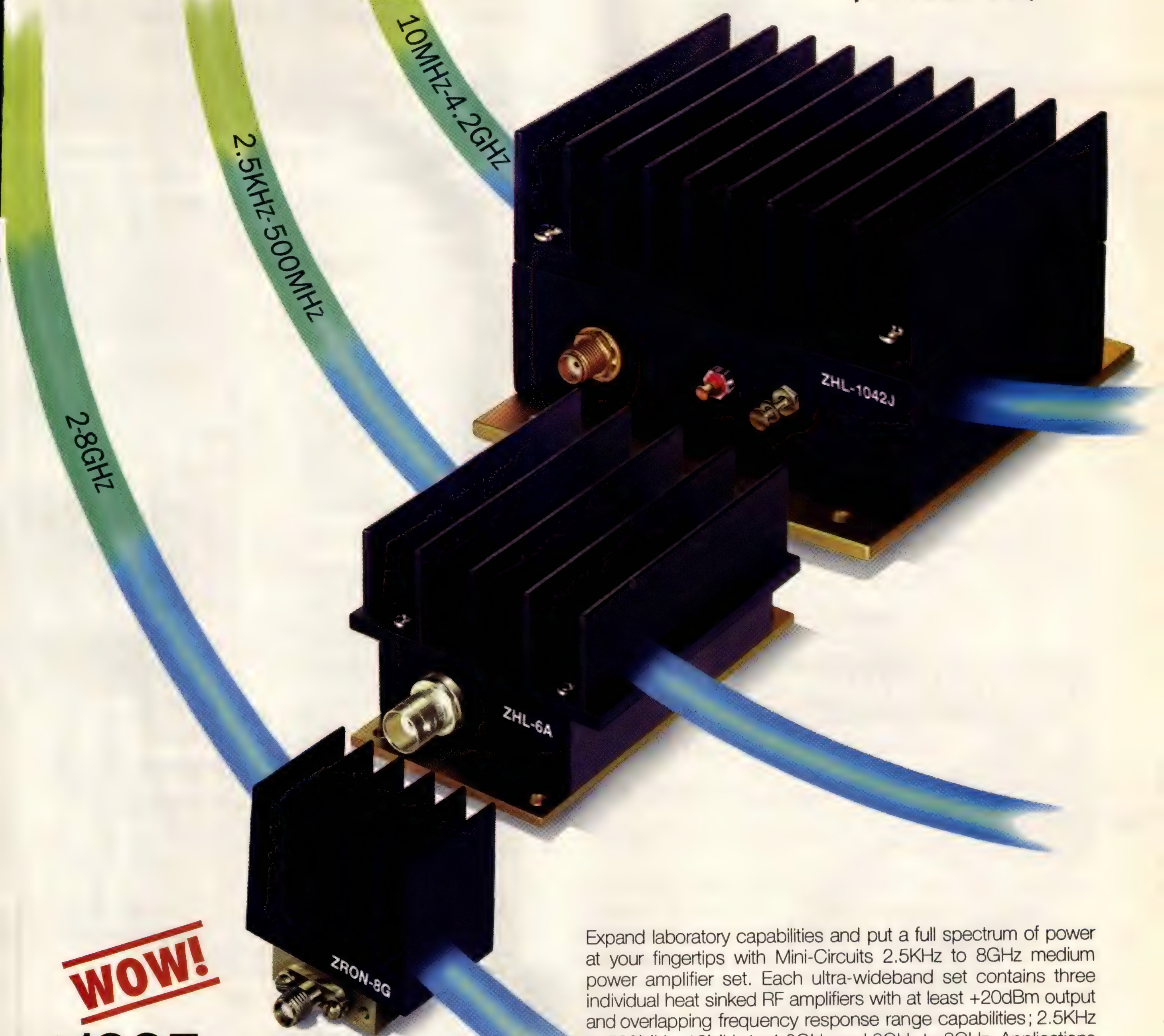

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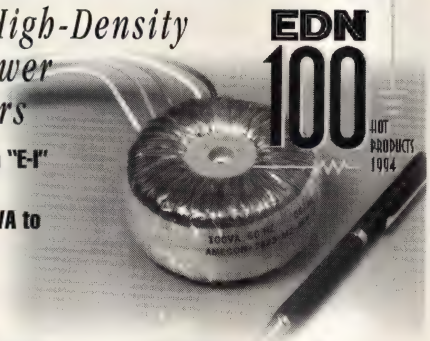

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LINEAR TECHNOLOGY

DESIGN NOTES

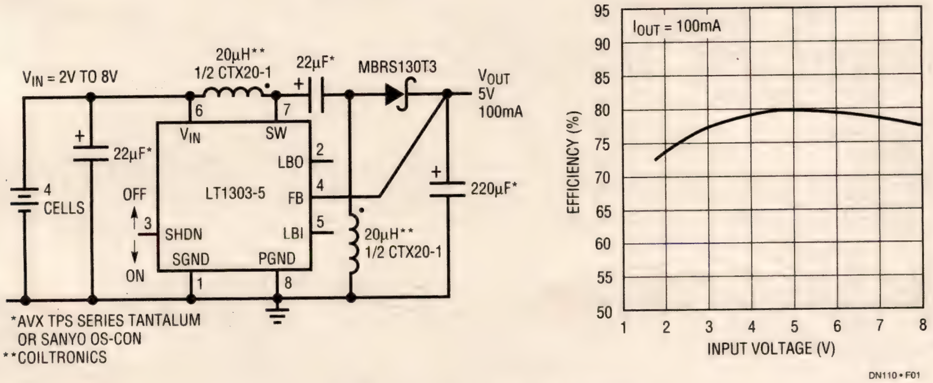
Micropower Buck/Boost Circuits, Part 2: Converting Four Cells to 5V* – Design Note 110

Mitchell Lee

Two combinations of cell count and output voltage are to be strictly avoided: three cells converted to 3.3V and four cells converted to 5V. These combinations are troublesome because no ordinary regulator (boost, buck or linear) can accommodate a situation where the input voltage range overlaps the desired output voltage.

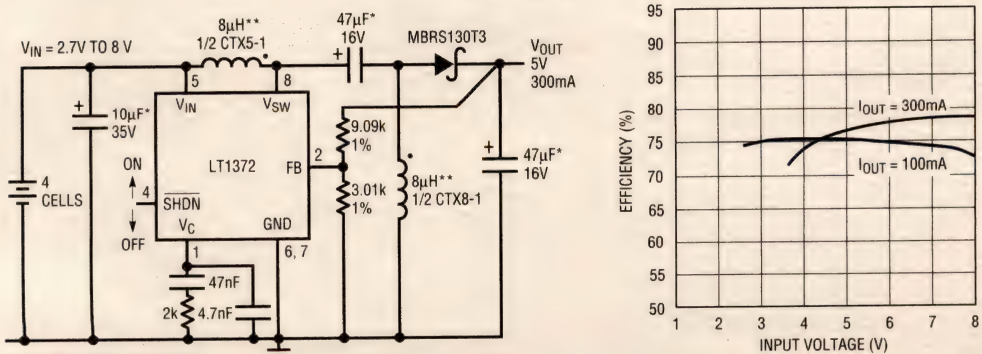
This design note presents four circuits capable of solving the 4-cell dilemma. Design Note 109 discussed 3-cell, 3.3V circuits. The LT®1303 and LT1372 high efficiency DC/DC converters are used throughout, giving a fair comparison of each topology's efficiency. The LT1303 is optimized for battery operation and includes a low-battery detector which is required to implement one of the topologies. The LT1372 500kHz converter is used for compact layouts at higher current levels.

You can expect 100mA output from LT1303 based circuits and 300mA from the LT1372 circuit without modification. All of the circuits feature output disconnect; in shutdown the outputs fall to 0V. The input range of LT1303 based converters extends well beyond the 3-cell source shown. These function at 1.8V, and although not fully characterized for efficiency, can accept inputs of up to 10V. The LT1372 converter operates from 2.7V to 10V.



V_IN = 2V TO 8V
20µH**
1/2 CTX20-1
22µF*
MBRS130T3
V_OUT
5V
100mA
6
7
V_IN
SW
22µF*
2
LBO
4
CELLS
OFF
LT1303-5
FB
4
220µF*
3
SHDN
5
LBI
20µH**
1/2 CTX20-1
SGND
PGND
ON
1
8
*AVX TPS SERIES TANTALUM
OR SANYO OS-CON
**COILTRONICS
I_OUT = 100mA
EFFICIENCY (%)
95
90
85
80
75
70
65
60
55
50
1
2
3
4
5
6
7
8
INPUT VOLTAGE (V)
DN110 • F01

Figure 1. 4-Cell to 5V SEPIC



V_IN = 2.7V TO 8 V
8µH**
1/2 CTX5-1
47µF*
16V
MBRS130T3
V_OUT
5V
300mA
5
8
V_IN
V_SW
10µF*
35V
9.09k
1%
ON
LT1372
FB
2
4
CELLS
4
SHDN
3.01k
1%
8µH**
1/2 CTX8-1
47µF*
16V
V_C
GND
OFF
1
6, 7
47nF
2k
4.7nF
*AVX TPS SERIES TANTALUM
**COILTRONICS
I_OUT = 300mA
I_OUT = 100mA
EFFICIENCY (%)
95
90
85
80
75
70
65
60
55
50
1
2
3
4
5
6
7
8
INPUT VOLTAGE (V)
DN110 • F02

Figure 2

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*For 3-cell to 3.3V buck/boost circuits, see Design Note 109.

The circuits in Figures 1 and 2 are based on the SEPIC (Single-Ended Primary Inductance Converter) topology. Although not stellar, the efficiency is quite consistent over a wide input voltage range. Peculiar to the SEPIC topology is its use of two inductors. These, however, are wound together on a single core and consume no more space than a simple 2-terminal inductor of similar rating. A wide selection of stock 2-winding, 4-terminal inductors are available from Coiltronics and other magnetics vendors.

Peak efficiency improves in Figure 3 using a bipolar buck/boost topology. This circuit is essentially a boost converter with a linear post regulator. For $V_{IN} < V_{OUT}$, the LT1303 boosts the input driving the bipolar emitter just high enough to maintain the desired output voltage—the transistor is saturated. For $V_{IN} > V_{OUT}$, the LT1303 drives the emitter to a value just higher than the *input voltage* sufficient to develop the base current necessary to support any load current. In this condition the transistor serves as a linear post regulator, cascoding the output of the boost converter and dissipating power as would any linear regulator.

Highest peak efficiency is obtained with the circuit in Figure 4 using a MOSFET buck/boost converter. For $V_{IN} < V_{OUT}$, the circuit operates as a boost converter and the MOSFET, driven by the LT1303's low-battery detector/amplifier, is held 100% ON. The output voltage is developed and controlled by the boost converter.

For $V_{IN} > V_{OUT}$, the boost function can no longer control the output voltage and it begins to rise. Staggered feedback (R3, R4, R5) allows the low-battery detector/amplifier to take control using the MOSFET as a linear pass element. Because the MOSFET requires no base drive, and because it has such a low ON resistance, the efficiency peaks at well over 90%. Furthermore, the efficiency peak occurs in the vicinity of a NiCd's nominal terminal voltage of 4 × 1.25 = 5V, right where the efficiency is needed most.

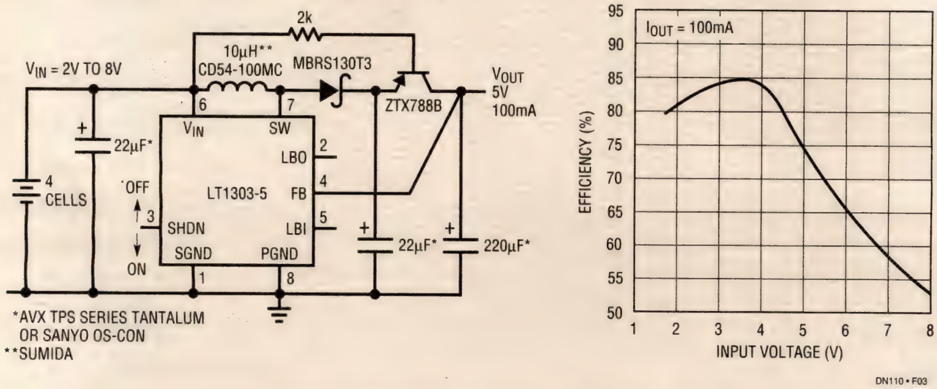
V_{IN} = 2V TO 8V
2k
10µH**
CD54-100MC
MBRS130T3
ZTX788B
V_{OUT}
5V
100mA
22µF*
4
CELLS
OFF
ON
LT1303-5
6
7
V_{IN}
SW
LBO
FB
SHDN
LBI
SGND
PGND
2
4
3
5
1
8
22µF*
220µF*
*AVX TPS SERIES TANTALUM
OR SANYO OS-CON
**SUMIDA
I_{OUT} = 100mA
EFFICIENCY (%)
95
90
85
80
75
70
65
60
55
50
1
2
3
4
5
6
7
8
INPUT VOLTAGE (V)
DN110 • F03

Figure 3. 4-Cell to 5V Bipolar Buck/Boost

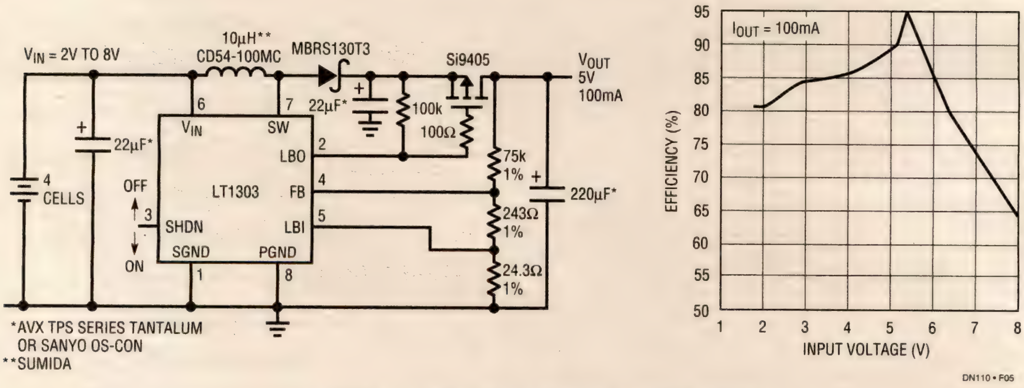
V_{IN} = 2V TO 8V
10µH**
CD54-100MC
MBRS130T3
Si9405
V_{OUT}
5V
100mA
22µF*
100k
100Ω
22µF*
4
CELLS
OFF
ON
LT1303
6
7
V_{IN}
SW
LBO
FB
SHDN
LBI
SGND
PGND
2
4
3
5
1
8
75k
1%
243Ω
1%
24.3Ω
1%
220µF*
*AVX TPS SERIES TANTALUM
OR SANYO OS-CON
**SUMIDA
I_{OUT} = 100mA
EFFICIENCY (%)
95
90
85
80
75
70
65
60
55
50
1
2
3
4
5
6
7
8
INPUT VOLTAGE (V)
DN110 • F05

Figure 4. 4-Cell to 5V MOSFET Buck/Boost

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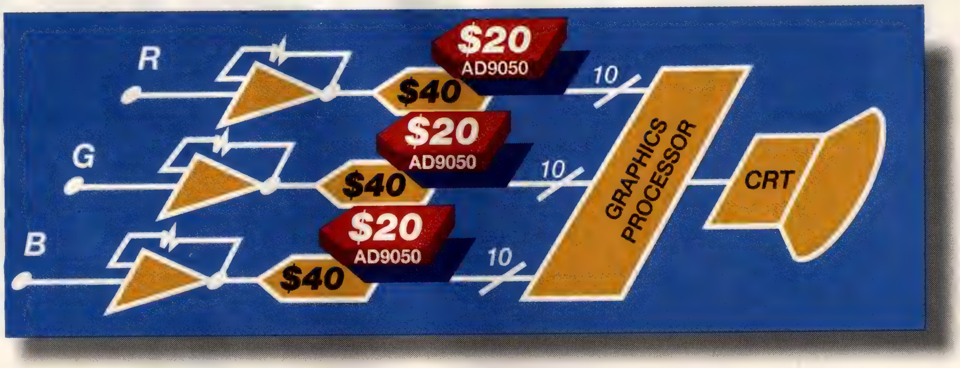

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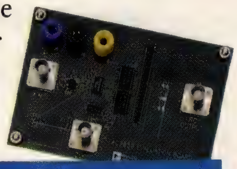

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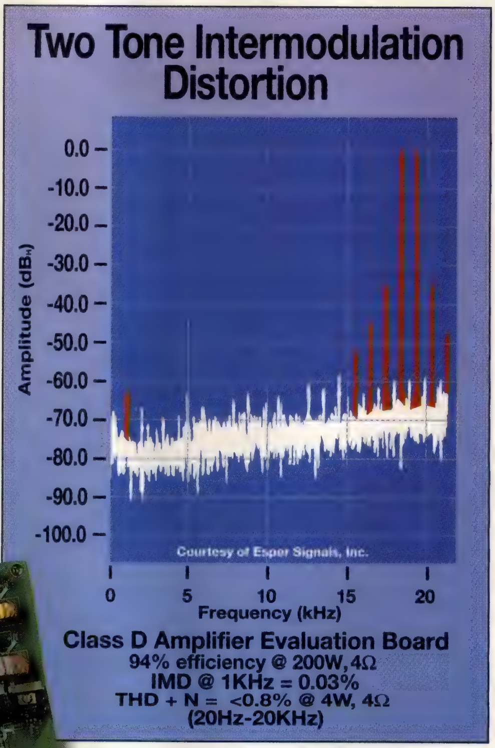

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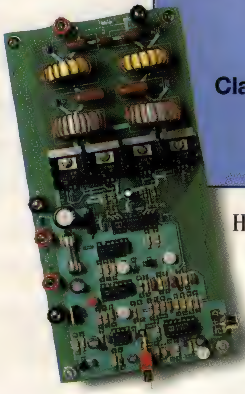

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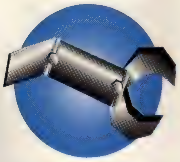


Live insertion of digital circuits requires knowing your IC family

JEFFREY B DAVIS, NATIONAL SEMICONDUCTOR CORP

It's often desirable—or even mandatory—for your system to allow "live" insertion and removal of circuit boards. Although digital-IC vendors say their ICs support this operation, there's no complete or easy solution to performing it without potential damage. You can get closer to this goal, though, by understanding live-insertion/removal perspectives and limitations, along with the differences among common logic families.

Systems for telecommunications, real-time transaction processing, and fault-tolerant computing must stay on-line during maintenance. For designers of such systems, the ability to perform live insertion and removal of boards has always been a desirable feature. More recently, the availability of open-architecture computing equipment, removable disk drives, and user-accessible backplanes and PC Cards has increased designers' needs for live-insertion/removable-capable devices.

Removing power from a module or board but leaving active signals connected to a bus or backplane causes a situation with fault conditions virtually identical to those of live insertion/removal. The difference is that, unlike live insertion/removal, your motive is to reduce system power consumption by idling unneeded subsections of the system. If the board or module contains CMOS drivers at its periphery, however, you achieve little in power savings. Standard CMOS devices with inputs or outputs tied to the bus attempt to power up and operate on this unintended supply, provided through their input-protection or drain-isolation junctions. Instead of benefiting from reduced power consumption, the subsystem may suffer data corruption, device damage, or circuit-board failure due to the large current flow this phantom-power condition causes.

Get the terms straight

You can divide live-insertion devices into classifications A, AA, and B (see **box**, "How tolerant are you?"). Each provides varying degrees of the following capabilities:

Data retention means that when you reduce the supply to a level below the guaranteed operating range and then return it to the allowed range, all internal storage elements and outputs retain or return to the values they had before the supply reduction. If the IC is to retain valid data, input, output, and I/O switching cannot occur during supply reduction or restoration.

Also, consider IC behavior during the various power-rail states. **Power-down, high-impedance** de-vices have inputs and outputs that present no dc load to applied external signals, even when the devices' supply voltage is nearly zero. Power-down high impedance is a requirement for Classification A devices.

Power-up reset means that the device's latches and outputs are guaranteed to be at valid and predetermined logic levels following application or reapplication of the supply rail. In a three-state power-up device, the outputs remain in a high-impedance condition during supply ramping and unconditionally return to the high-impedance condition when the supply drops below the power-up threshold. The IC's design prevents the outputs from becoming active until the supply rises to a predetermined threshold level. This situation, in turn, prevents the IC from presenting invalid data at its outputs. In addition, inputs are internally conditioned via bus hold or externally driven via pull-up resistors to the ramping supply.

Input-bus-hold hysteresis lacks the usual buffering between the feedback-device output and the input pin. The purpose of bus hold is to establish a valid, or safe, input level on otherwise-floating inputs. More circuit designers are trying to use the bus-hold output-low or output-high current to act as the termination supply, but bus hold does not suit this application.

Each family is different

Although most circuit designers don't worry about the details of internal IC circuitry and topology, an effective design for live-insertion/removal requires that you understand how these structures affect what you can expect.

Standard CMOS-logic devices, including the CD4000, HC/HCT, ACT, and LV families, fit the live-insertion/removal-intolerant definition. These devices use complementary input-protection junctions to provide ESD immunity (**Fig 1a**). The input-to-V_{DD} P+/N– clamping diode, D_1, creates a live-insertion/removal obstacle because it becomes forward-biased whenever you apply a positive-going signal to an input if you do not apply V_{DD}. This scenario assumes that a floating V_{DD} node discharges nearly to ground potential. This approach results in a low-impedance path from the input node to V_{DD} and subsequent failures of input leakage current.

Live insertion/removal causes forward, or avalanche, junction currents. These currents develop potential differences in the substrate and local wells of the device as charge escapes to the supplies. This scenario differs from that of well-controlled channel and drift currents that are inherent with conventionally operated MOS devices. In an N– starting-material CMOS process, the P– well forms the base of a relatively high-performance parasitic vertical npn, and the substrate represents the base of the lateral pnp. In this process, any local potential differences in the N– substrate or P– well inadvertently provide the forward voltage to turn on these parasitic bipolars. SCR triggering or latch-up may result.

For the output circuit of a standard CMOS logic device, you typically use a large PMOS pull-up transistor to provide large, high-level output current and large noise margin. (**Fig 1b**). The drain-isolation P+/N– junction inherent to these PMOS transistors must remain reverse-biased to preserve proper device operation. Unfortunately, you forward-bias this junction if you apply any signal >V_{DD} to the output when V_{DD} is ~0V or any signal >V_{DD}+ the forward drop across the diode.

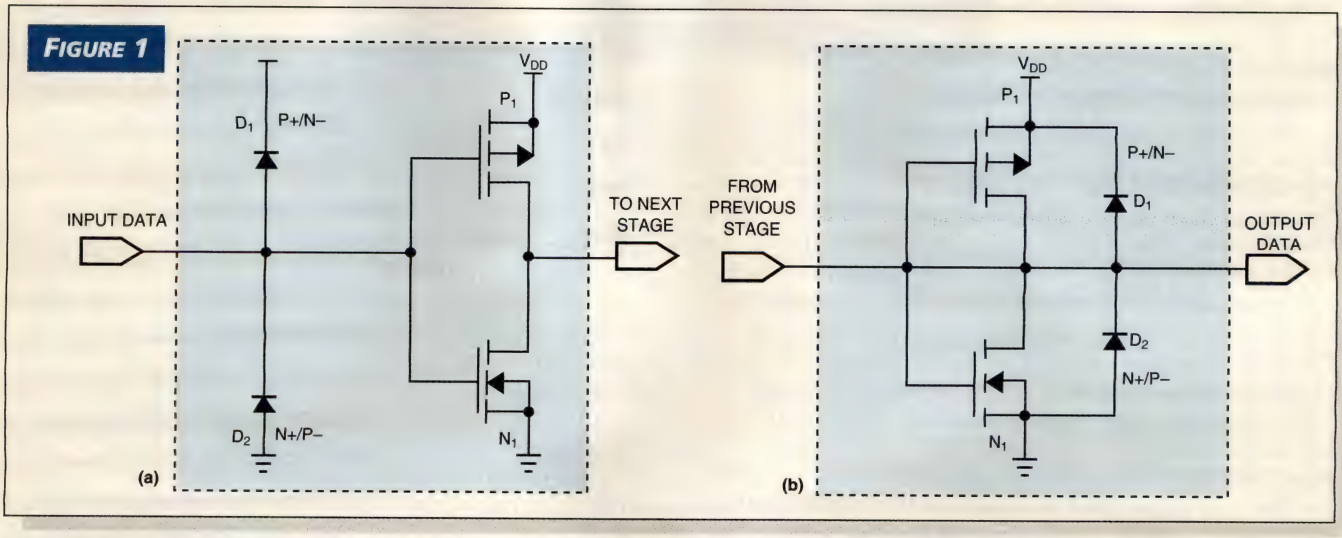
As a result of these high-current conditions, the device may have behavior ranging from a subtle shift in dc characteristics to compromised reliability, which is unapparent at the time of the stress, through catastrophic failure. You may see outputs do one or more of the following: glitch low-high-low as V_{DD} rises, remain low, glitch low-high and then collapse to and track V_{DD} as it rises, glitch low-high and oscillate, or fail outright.

Unfortunately, you can't predict or reliably repeat the live-insertion/removal behavior for a device or for a class of devices. The actual behavior depends on factors such as dc-junction leakage, parasitic capacitance, and other environmental conditions, such as the presence of external electric and magnetic fields and supply and ground noise.

Input overvoltage-tolerant CMOS devices, including VHC, LVX, LVC, and FCT types, have no P+/N– junctions between their input node and V_{DD}. (LVC's inclusion in this group is questionable because its data sheets specify an absolute maximum high-level input voltage level of 4.6V, so that you cannot apply 5V signals to LVC inputs.) The lack of these junctions lets you apply input signals containing voltage components >V_{DD}. When V_{DD} is ~0V, which is the case just before live insertion/removal, any positive-going signal that you apply to the input contains components >V_{DD}.

The input overvoltage tolerance of these devices is due to the lack of an upper diode in their input structure (**Fig 2**).

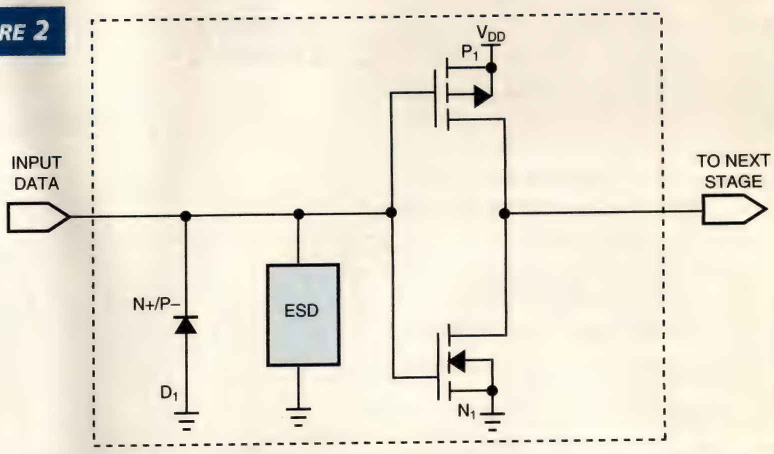
FIGURE 1



In a simplified standard CMOS input (a), the input-to-V_{DD} P+/N– clamping diode, D_1, creates a live-insertion/removal obstacle because it becomes forward-biased whenever you apply a positive-going signal to an input if you do not apply V_{DD}. For the output circuit of a standard CMOS logic device (b), you typically use a large PMOS pull-up transistor to provide large, high-level output current and large noise margin.

These devices have Classification B live-insertion/removal performance. Unfortunately, this classification often comes at the expense of compromised positive-ESD immunity. The ESD block in **Fig 2** represents the alternate positive-discharge-protection element. This alternate circuit does not include a forward path to V_{DD} but instead routes positive discharges to ground. To implement the alternate-ESD scheme, logic vendors use different circuitry, including reach-through NMOS transistors, gateless NMOS, field-threshold NMOS, grounded-gate NMOS, zener diode, floating-base npn, and others.

FIGURE 2



CMOS input circuits have overvoltage tolerance due to the removal of the upper diode in their input structure.

The common feature among this group is the absence of a forward path from the input node to V_{DD}. From a live insertion/removal point of view, the output circuits in this class are identical to the standard complementary MOS output circuit in **Fig 2**.

Tristated output overvoltage-tolerant CMOS/BiCMOS, a relatively new class of CMOS or mostly CMOS logic, includes LCX and LVT devices. These devices have inputs and outputs that present a high-impedance load to the host system at both the devices' inputs and outputs when V_{DD} is not applied. In addition to the alternate input structure, these devices feature novel CMOS output circuitry that tolerates the application of output voltages $>V_{DD}$, with $V_{DD}\sim 0V$ or an output in tristate mode, without substantially increasing high-level, high-impedance leakage current. Product lines fitting this description include the Motorola/National/Toshiba LCX low-voltage family and the Texas Instruments LVT low-voltage BiCMOS logic. These products offer Classification A live-insertion/removal tolerance.

In an overvoltage-tolerant input circuit (**Fig 3**), P_1 and N_1 provide hysteresis by routing feedback directly to the input node. This technique contrasts to the usual technique, in which you apply the feedback one stage further into the buffer to avoid back-driving the bus. In this approach, directly charging the input is desirable because it establishes a valid level to the input inverter, P_2 and N_2, when the bus is

HOW TOLERANT ARE YOU?

When you're dealing with live, or "hot," insertion/removal, you are electrically completing data, clock, control, or supply connections to a device with no regard for proper sequencing or signal stability. Because this scenario can have different implications on various devices, the industry has established several levels of tolerance.

Live-insertion/removal-intolerant devices may fail, compromise reliability, or damage host-system pc-board traces when inserted into an electrically active system. The failure may be evident only during the insertion itself, or damage may occur that causes the device no longer to satisfy its ac or dc guarantees. Such insertion can also degrade data integrity within the device and on the bus. Successful use of this class of product in live-insertion/removal applications requires significant effort and, probably, additional components.

Live-insertion/removal Classification B devices differ from the intolerant class due to their input structures, which present no dc load to an active host bus when there is no power supply to the device. These devices preserve data integrity on a host bus exposed only to device inputs while there is no device supply. These devices require external circuitry to provide the necessary sequencing of ground, supply, and signal connections to output or I/O pins, and you may need to reboot the system to configure and initialize all affected hardware following a live insertion.

Live-insertion/removal-tolerant Classification A devices satisfy Classification B requirements, and, in addition, their output pins present no dc load to an active host bus when the device's supply is not applied. These devices also preserve data integrity on the host bus when the device supply is not applied. Input pins require pull-up resistors or equivalents to hold off outputs during the supply rise time, and these devices require retransmission of data to the inserted subsystem.

Live-insertion/removal-tolerant Classification AA devices satisfy Classification A requirements, and their output pins remain in a high-impedance state until valid data is set up at the output predriver. This approach preserves data integrity on the host bus and within the device. Classification AA devices may allow you to do live insertion/removal without external support circuitry. You may also have to retransmit data to the inserted subsystem.

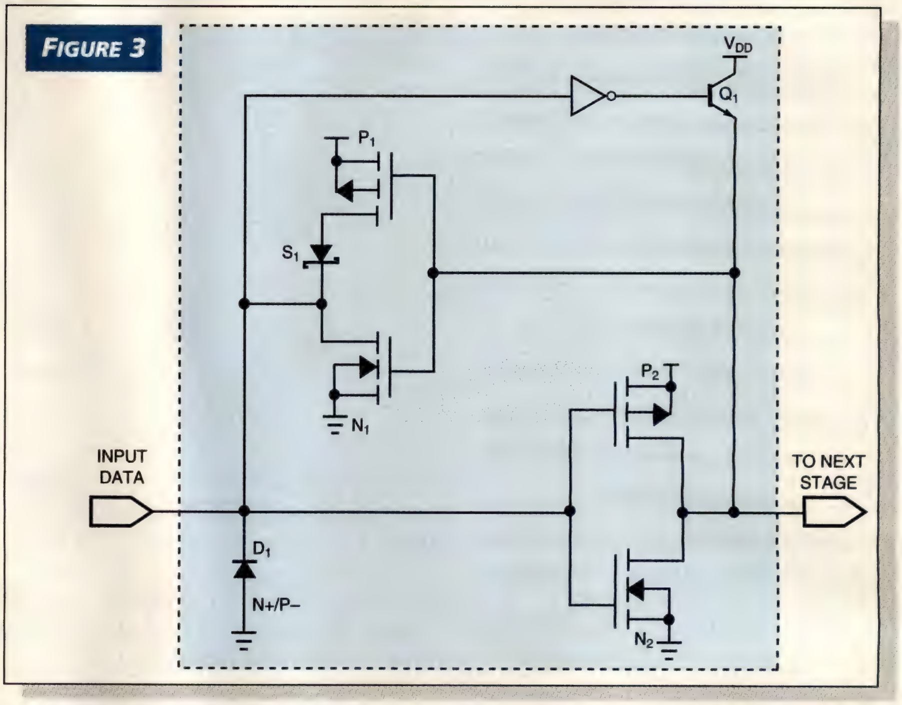
floating or otherwise indeterminate. Reverse-biased Schottky barrier diode S_1 prevents the corruption of the 3V supply in the event that the input charges above the static V_{DD} level. Without S_1, the drain-bulk P+/N– junction of P_1, would be forward-biased when V_{IN} rises above V_{DD} plus the forward diode drop at P_1.

In an overvoltage-tolerant output circuit (**Fig 4**), analog multiplexer X_1 passes on the larger of V_{DD} or V_O. These devices thus isolate V_O from V_{DD} and tolerate overvoltage conditions. When V_{DD} is ~ 0, these devices treat any signal greater than that at the output as an overvoltage condition.

CMOS/BiCMOS with power-up/down, high-impedance devices relates closely to the overvoltage-tolerant families but includes circuitry (the components with * in **Fig 4**) to prevent outputs from activating whenever V_{DD} is below a predetermined level. These Classification AA live-insertion/removal products include ABT and LVTZ devices.

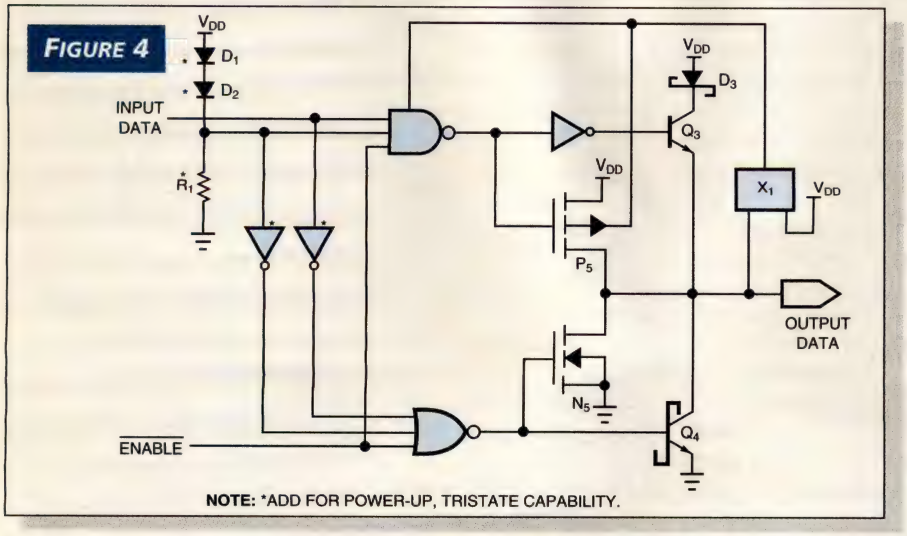
This extra circuitry prevents invalid or electrically unusable signals that develop during the supply-settling time from presenting to the host bus or other inputs. The extra logic in the output predriver overrides the enable signals that are otherwise delivered to complementary output pairs as long as diodes D_1 and D_2 remain reverse-biased. This approach effectively holds the outputs in the high-impedance condition until V_{DD} rises to a level equal to or greater than twice the forward voltage of D_1.

FIGURE 3



Routing feedback directly to the input node provides hysteresis in this simplified, overvoltage-tolerant, BiCMOS input circuit with bus hold.

FIGURE 4



NOTE: *ADD FOR POWER-UP, TRISTATE CAPABILITY.

In an overvoltage-tolerant BiCMOS output circuit, adding the components with * creates an output circuit with power-up, tristate capability.

Analog NMOS switches can be implemented without P+/N– junctions between any pins and V_{DD} (**Fig 5**); examples include Quality Semiconductor's QuickSwitch series, Texas Instruments' CBT family, and National Semiconductor's BusSwitches. These devices generally offer the same live-insertion/removal capabilities as LVT and LCX devices. The critical live-insertion/removal constraint with these devices is that the input levels—or control inputs in the case of the NMOS switches—must remain at valid levels during supply power-up. You can most easily accomplish this goal by using active termination or input pull-up resistors.

The ESD block in **Fig 5** represents the alternate positive-ESD element. Similar to that of **Fig 2**, this protection circuit does not include a forward path to V_{DD}; instead, it routes positive discharges to ground. These devices meet the requirements for Classification A live-insertion/removal tolerance.

Extended TTL (ETL) technology is a VME-compliant, high-drive logic family featuring overvoltage-tolerant inputs and outputs and additional functionality to improve live insertion/removal support. A "connect-first" pin, $V_{DD\,BIAS}$, precharges the host-side outputs to 1.5V to minimize the disturbance of sudden charging or discharging of the inserted ETL pins. As with LCX and LVT devices, you must

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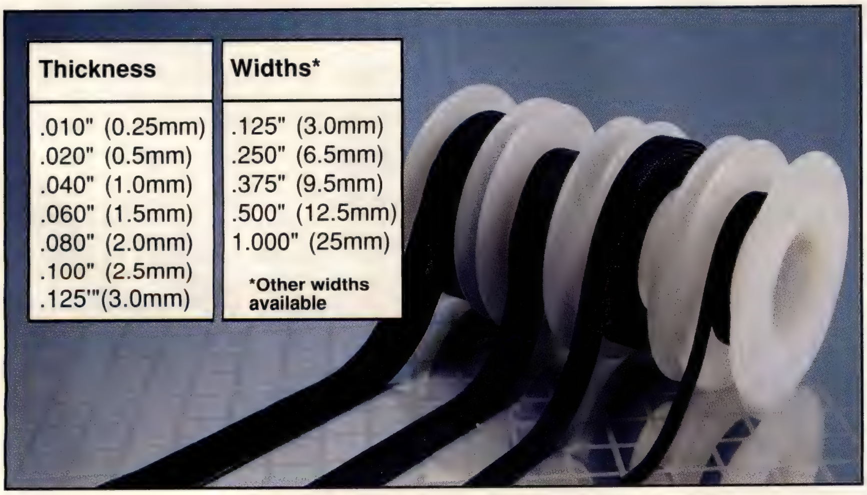

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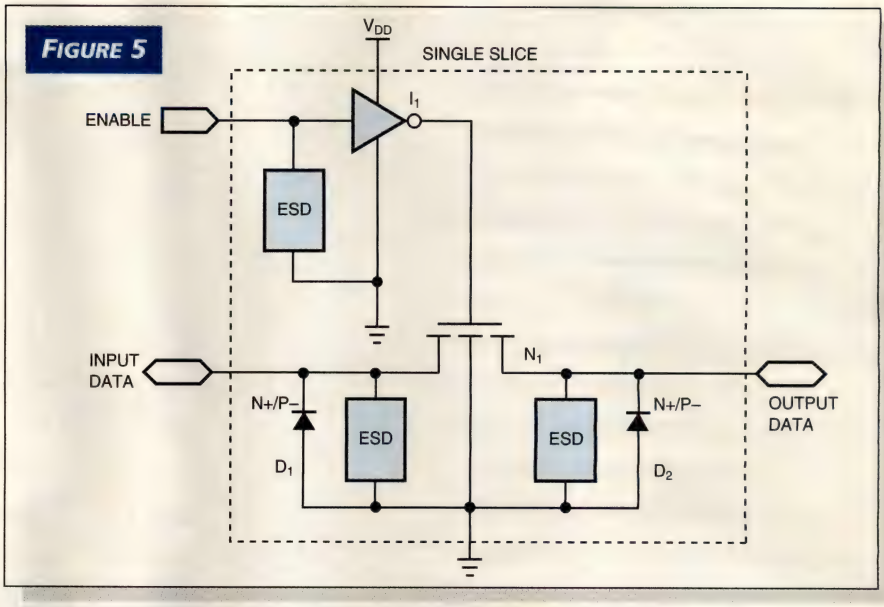
CIRCLE NO. 50

hold the control inputs at valid levels during supply power-up. You can most easily achieve this goal with active termination or input pull-up resistors. ETL fits the description for Classification A live-insertion/removal performance.

FIGURE 5



An NMOS switch circuit lacks P+/N– junctions between any pins and V_{DD}.

Applying system-level techniques

Bus standards, such as the VME64 ETL specification, include specifications for the mechanical keying of modules or subsystems for insertion into live systems. By arranging the order in which you apply power-supply connections, signal connections, and precharge connections to a live-inserted component or subsystem, you avoid certain fault conditions. You can circumvent the problem of temporarily forward-biasing input-protection diodes or PMOS drain-isolation junctions by extending the supply connectors so that they make contact with the backplane before any signal lines do.

You can't make pure CMOS devices unconditionally live-insertable/removable solely by implementing supply/signal sequencing. Keying does eliminate the undesirable forward-biasing of the P+/N– input-protection diode and drain-isolation junction inherent to the output PMOS transistor. However, power-up of a CMOS-logic device without establishing valid input levels frequently results in a potentially destructive, high-current condition due to high-frequency oscillation, along with simultaneous conduction through the input complementary pair. Several unpredictable external and internal factors determine whether "hazardous" input levels exist at an otherwise-floating input during live insertion/removal. These factors include

- the voltage that the floating input reaches, due to the divider formed by the ratio of input P+/N– junction leakage to V_{DD} and N+/P– leakage to ground
- the presence of terminating networks or pull-up resistors on the input nodes
- the input capacitor's precharged condition
- the static-charge buildup on the subsystem or host
- the ratio of subsystem input leakage to host stray capacitance
- the presence of radiated electromagnetic energy.

You can eliminate the hazards associated with indeterminate inputs when power is applied by using ICs with internal circuitry that sets otherwise-floating inputs to valid levels as soon as power and ground references are available. Two product families featuring circuitry to perform this function—National Semiconductor's dual-supply LVX4245 (B-port only) and Texas Instruments' LVT low-voltage BiCMOS logic family—apply hysteresis directly to the input node, such that under no- or light-load conditions, the input charges or discharges to a valid input level.

Use pull-up resistors to set floating LCX or LVT control input pins to valid levels and avoid problems with outputs leaving tristate mode before you establish proper predriver levels.

By combining careful circuit design with classification A or AA logic, you can develop an acceptably robust and reliable live-insertion/removal subsystem or module. If your application is cost-sensitive at the component level but has extra board space, you have to accommodate live-insertion/removal at the system-design level. By using external, active- or ac-termination schemes, you can use lower cost, less sophisticated standard logic devices without compromising live-insertion/removal requirements. In contrast, for applications where space savings is critical, look at the advanced logic families that feature built-in live-insertion/removal enhancements. Most applications require some external circuitry to allow unconditional live insertion/removal of subsystems. EDN

Author's biography

Jeffrey B Davis is a design engineer at National Semiconductor's Data Management Division, South Portland, ME. He has a BSEE from the University of Wisconsin—Milwaukee and is chairman of the EIA/JEDEC JC-40 Digital Logic Committee.

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CIRCLE NO. 67

(AS FOR THE VERY SHORT WORK WEEK, WE DO HAVE A SMALL SKUNKWORKS LOOKING INTO IT.)

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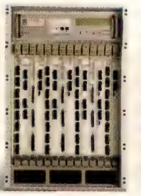

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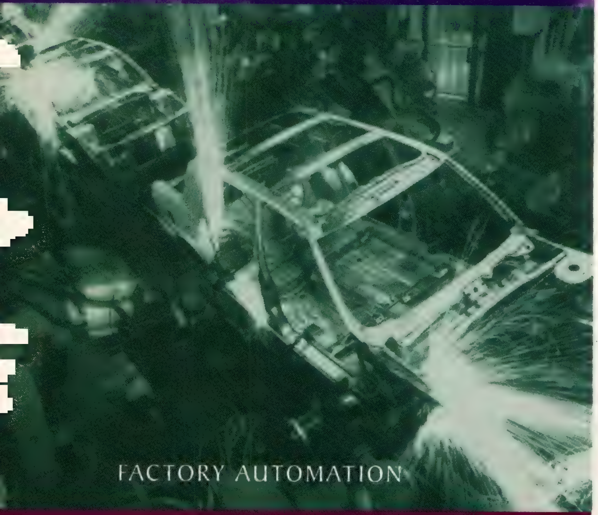

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CIRCLE NO. 54

Use performance modeling to predict and minimize flex cable catastrophic failures

PAUL WARREN AND TOM ROSENMAYER, WL GORE & ASSOCIATES INC

The mechanical limitations of cabling systems can easily compromise increasingly sophisticated industrial electronics. By using test and modeling techniques reserved for higher level components, you can overcome most of cabling systems' common failure modes.

Cabling, particularly in flexing systems, has been a problem for system designers. System designers must provide the reliability required to maintain productivity while responding to the increased use of automation. Flex cables, often misperceived as low on the technology food chain, have a direct impact on the reliability of equipment. Their failure can instantly neutralize all electronic and mechanical functions, bringing entire production lines to a standstill.

Because of the importance of constant uptime to lean production scheduling, system designers are applying more sophisticated evaluation techniques, such as Weibull charts, to their flex cable design. Although designers often use these charts to illustrate fatigue failure in electronic components, you can apply them to flex cables to go beyond typical "flex-cycles-to-failure" data. The charts more accurately pinpoint the expected failure levels of a given flex cable. Understanding failure profiles and their underlying basis allows you to take appropriate precautions in the design stage. You can, thus, avoid production-stopping cable failures.

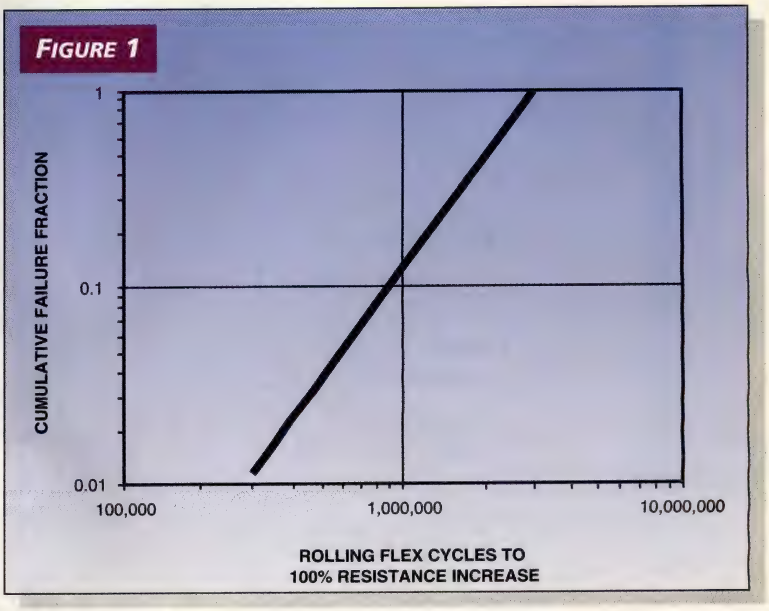
Failure modeling using Weibull plots

Designers often use reliability statistics to characterize the lifetime of complex electronic components that are subjected to stress, such as ICs and pc boards. Also, designers routinely use Weibull distribution plots to calculate the reliability of ICs but have never applied them to flex cable systems. By using this more sophisticated analysis, you can gain insight into expected failure plateaus for cabling components.

Fig 1 shows a Weibull distribution for a flex cable with the cumulative failure fractions over a range of rolling flex cycles. Once you establish the distribution, you can calculate the system lifetime to a certain level of confidence. For example, from the plot in **Fig 1**, you can see that more than 95% of the cables will last a minimum of 500,000 cycles.

Traditional data for flex cables provide only a minimum

FIGURE 1



Weibull plot of 38 test-to-failure runs of FAC-type flex cable shows that more than 95% of the cables last at least 500,000 cycles, where failure is defined as a 100% increase in resistance.

bend radius, with no average lifetime or distribution. Therefore, you can't make accurate predictions about reliability. A statistically valid Weibull plot for flex cables should contain data from at least 20 actual stress-to-failure tests. Designers have not used stress-to-failure tests because of the expense. However, a serious analysis of performance demands this commitment level. **Fig 1** shows 38 separate runs of the stress test.

By applying this analysis and other advanced statistical tools to the design of flex cables, you can get a more accurate determination of MTBF, which affects service scheduling. You can apply these models to a number of design parameters. The combination of modeling and detailed design knowledge results in a significant increase in the reliability of flex systems.

Causes of failure

You can segment the flexing of cables into the three basic motions (**Fig 2**). Each time you bend or flex a cable, you stress the copper conductors and shields. Copper has poor resistance to repeated stressing and can fatigue and fail even if the stress is kept below its ultimate yield point of 15% elongation. Copper has low resistance to shear stress because of its different crystal structure. The metal can deform even if the stress is below the plastic yield point. (In contrast, steel does not deform because of its crystal structure. Instead, steel springs back to its original position each time it is stressed below its plastic yield point.)

Cable that is subjected to flexing can fail for three reasons: cable and conductor insulation degradation, conductor and shield fatigue in flex area, and conductor and shield fatigue at point of termination.

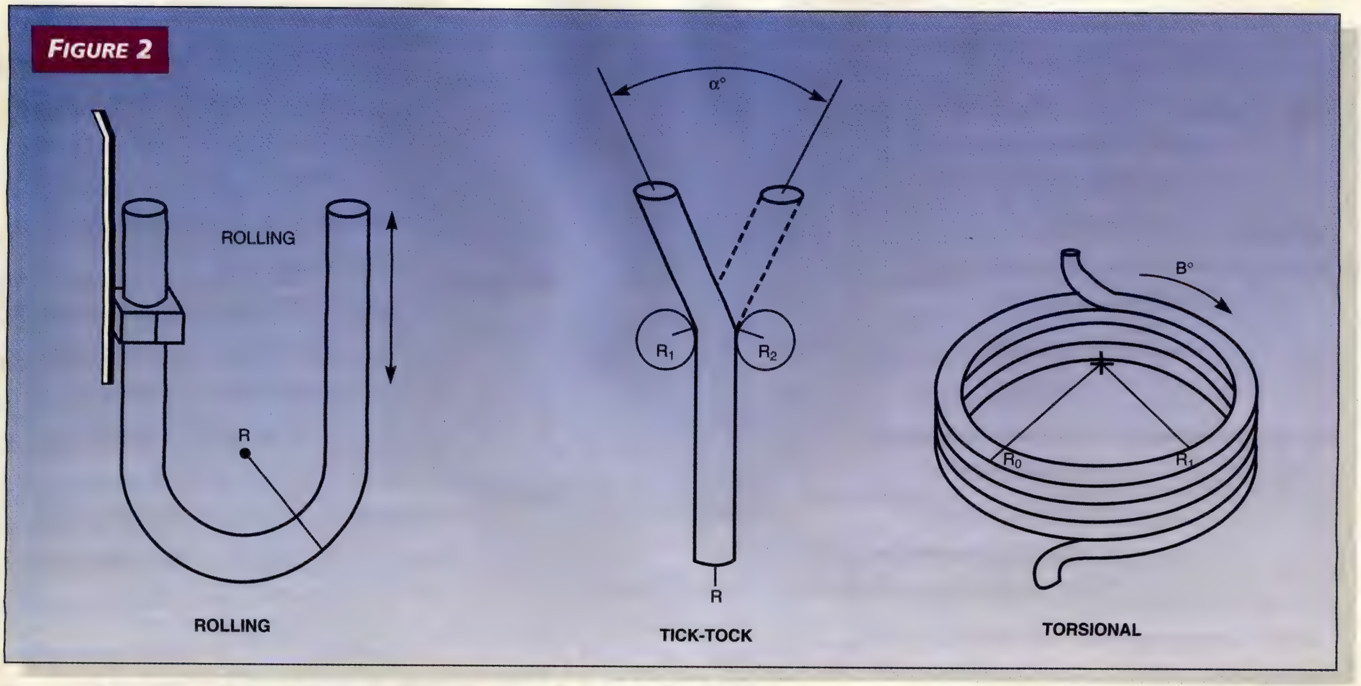
Insulation and jacket degradations. Cable insulation or cable-jacket failure is caused by constant abrasion between the cable and other cables, hoses, or cable-management hardware, such as cable tracks. Metal or plastic chips, solvents, and lubrications can also contribute to rapid degradation of the cable insulation. When the cable jacket fails, it exposes the cable interior. Any liquid that is present works its way into the cable and eventually causes a short circuit between the conductors. Abrasive particles can also attack the conductor insulation and cause it to fail. If the cable has an overall shield, it opens to ground. **Table 1** shows the jacket materials resistant to abrasion.

Another physical property to consider is tensile strength. You can use a thinner jacket if the tensile strength is high. Jacket size is an important factor to consider when trying to reduce the size of the cable bundle.

Temperature extremes and low atmospheric pressures (vacuum) weaken or embrittle the cable jacket. You should select a jacket material that is rated for the operating temperature and does not contain plasticizers. Plasticizers evaporate over time or at low pressures and cause the jacket to embrittle.

In addition to meeting the same requirements as the cable insulation, conductor insulation must resist crushing. In a typical round cable, clamping or flexing a cable in a track with many cables and hoses exposes the conductors to high compression forces. Insulation with high tensile strength and low elongation, such as polyester, is best for most industrial applications. If you're managing a large number of conductors in a small area, a thin-wall, high-strength conductor insulation reduces the size of the cable and has the greatest effect.

FIGURE 2



You can have three distinct degrees of motion in a flex-cable application.

Conductor and shield fatigue in flex area. The most common mode of cable-flex failure involves the eventual fracture of the conductor in the flex area (**Fig 3**). The conductors are still functioning when the shield fails, so the operation continues. The cable is susceptible to EMI/RFI and emission, however. This situation creates errors and false signals with a source that is difficult to identify—typical of EMI/RFI problems.

To understand the mechanism of conductor and shield failure, look at the basic concepts of stress analysis. A rigid body's resistance to bend depends on the material, shape, and area of the cross section and radius of curvature of the bend. This stress, σ, is represented mathematically by:

$$\sigma = Mc/I,$$

where M=bending moments, c=distance from the neutral axis of the body to any fiber in the cross section, I=moment of inertia of the cross section, and σ=stress in the fiber at distance c.

For a typical flex cable, the geometry of the bend is fixed by considerations that include mechanical-design constraints and package layout. You must work within these constraints and minimize the conductor stresses that reduce

TABLE 1—CRITICAL PHYSICAL PROPERTIES OF POLYMERS FOR INSULATION AND JACKETING

Gore part number		**J-380**	**J-210**	**J-100**	**J-1315**	**J-365**	**J-363**	**J-1280**	**J-601**
General material class		**Thermoplastic rubber**	**Urethane**	**PVC**	**Thermoplastic rubber**	**Polyester elastomer**	**Polyester elastomer**	***PVDF***	***Gore-Tex* expanded PTFE**
Physical properties	**Units**								
Specific gravity	G/CC	1.13	1.25	1.31	1.24	1.20	1.22	1.78	0.60 to 0.80
Tensile strength	PSI	1675	4000	2450	1050	6400	6400	5000	>5000
Elongation	%	530	600	325	410	560	440	500	>50
Abrasion resistance		Fair	Excellent	Good	Fair	Excellent	Excellent	Good	Fair
Compression resistance	%/C	30/25	27/23		29/25	<1/23	<1/23		
Useful temperature range	°C	–40 to 135	–73 to 85	–55 to 105	–45 to 135	–30 to 125	–20 to 125	–30 to 150	–273 to 260
Melting point	°C	190	140	185	190	218	214	240	327
Coefficient of thermal expansion	10^{-5}/C	19	10	5 to 25	20	6	6	8	
Limiting oxygen index	%	23	32 (22 without FR)	29	21	22	22	42	>95
Flammability (UL)		94 H-B	94 V-O	94 V-O	94 V-O	94 H-B		94 V-O	94 V-O
Durometer shore A or D		38D	86A	86A	80A	55D	63D	65 to 70D	
Radiation resistance		Fair	Good	Good	Fair	Good	Good	Good	Poor
Chemical resistance		Good	Good	Fair	Good	Very good	Good	Good	Excellent
Tear	LB/IN	369	103, (D470)		194	Die B, 935	Die B, 1055		
Electrical properties									
Dielectric constant		2.42	7.0	5.0	2.44	4.6	4.4	8.0 to 10.0	1.3 to 1.7
Dielectric strength (short)	V/MIL	500	500	500	500	400 (0.075 in.)	410 (0.075 in.)	280	50
Volume resistivity	OHM-CM	10^{16}	10^{11}	10^{12}	10^{16}	10^{10}	10^{11}	10^{14}	$>10^{18}$
Arc resistance	SEC	0.79				0.04	0.04	0.04 to 0.09	
Typical applications		•Catalog cables •Excellent general-purpose jacket •High temperature •Excellent flex life	•Abrasion •Nuclear •Flexible	•General purpose •Flexible	•Very flexible •High temperature •Excellent flex life	•High abrasion •High temperature •Coils •Stiff/hard	•High abrasion •High temperature •Coils •Stiff/hard	•Clean room •Very pure	•High temperature •Excellent flex life •Excellent chemical resistance •High lubricity •Inert •Clean room

FLEX CABLE APPLICATIONS

flex life. To reduce the fatigue on the copper conductor and shield and, therefore, eliminate wire breakage, you should make the bend radius as large as possible. The diameter, or thickness, of the cable should be as small as possible.

The most important factor in determining flex fatigue life is the maximum stress in any part of the cable. Assuming the bend radius does not go below a minimum value, this maximum stress, R_{MIN}, is given by:

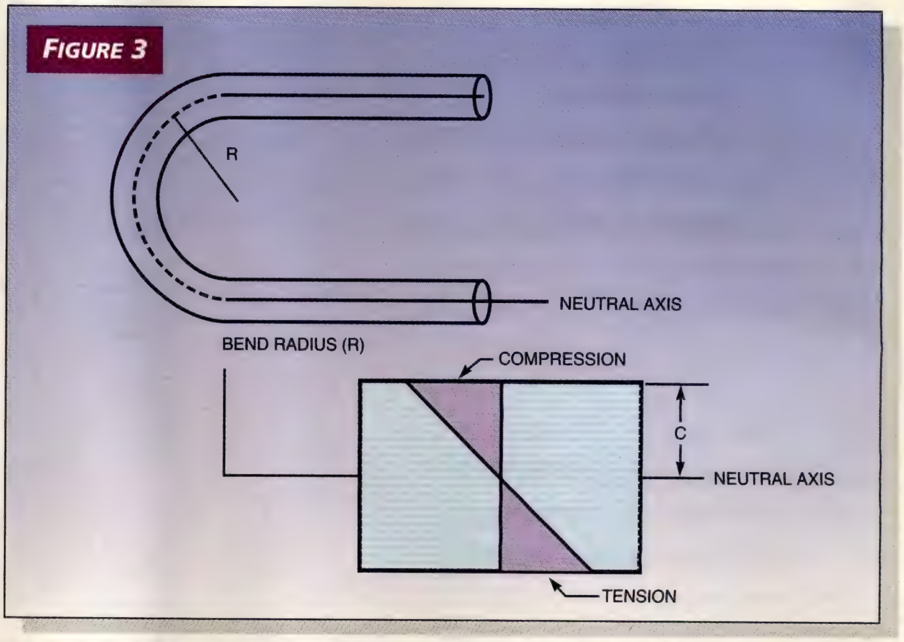
$$\sigma_{MAX}=E_{C_{MAX}}/R_{MIN},$$

where E=modulus of elasticity in psi (17million for ETP copper), C=maximum distance from the neutral axis to any fiber, and R=bend radius. Notice that this relationship holds for any cross section because the moment of inertia, "I," does not appear.

You can minimize stress by decreasing the cable thickness, or diameter, C_{MAX}, or by increasing the bend radius, R_{MIN}. You can also select conductor and shield materials of higher tensile strength than copper.

Flexing tests show that the resistance of the copper conductors and shield increases as the metals work harder under flexing. The harder you work the metal, the more brittle it becomes. Faster cycle rates of the equipment generate greater temperatures in the copper. A small bend radius also creates a higher temperature as well as a higher degree of fatigue. The increased temperatures can create insulation softening. The insulation softening changes the insulation's physical properties, such as reduced abrasion resistance, decreased cut-through resistance, and decreased tensile strength. Therefore, all of these changes can cause premature cable failure.

FIGURE 3



Cross-sectional analysis shows the stress points of a flexing cable.

Conductor and shield fatigue at the point of termination. Bending stresses and vibration from moving cables cause connectors and crimped or soldered cable terminations to break. Unsupported cables prematurely fail because of fatigue at the connector interface. You should always clamp flexing cables to a rigid surface at the point of termination to remove any stress from the termination points. Your choice of the proper strain-relief method is as important as the proper selection of insulation and conductors. Cables can suffer "whiplash" from fast-moving carriages, which cause the cable to change direction quickly and snap. In all high-speed flexing applications, a cable that is stiff offers resistance to bending. A stiff cable flexes much longer than a limp cable, which offers little resistance to bending and results in the whiplash phenomenon.

Design for failure prevention

To increase flex life in cables, you need to consider size carefully. By reducing the diameter of the cable, you achieve an exponential increase in flex life when the bend radius is held constant. Using standard copper conductors and reducing the size and weight of the cable can increase flex life (reliability) and reduce costs. By starting with a conductor insulation that has high dielectric strength and good tear-resistance characteristics, you can use insulation thickness 50% thinner than current insulations. Standard insulations that are voltage-rated at 300V rms for 0.004-in. wall thickness are available. (One example of this type of insulation is the MIL-ENE from WL Gore & Associates.) Reducing the conductor insulation thickness decreases the overall diameter of the finished cable.

You should also consider the lay-up of typical industrial cables, which designers often ignore. Each manufacturer has a process that seldom varies. Nevertheless, lay-up is one of the most critical processes to increase the flex life of round cables. The vendor can adjust the lay of the cable, the twists per inch of the conductors, and the conductor lay to optimize cable reliability for flex applications. Cable manufacturers with proven understanding of flex cable requirements develop cable processes with optimum lay-up to maximize the cable life. If done properly, this process has a significant impact on reliability.

Reducing the diameter of the cable results in an exponential increase in flex life at a given bend radius. The cable shield is often the first component to fail. The shield is at the greatest distance from the neutral axis of the cable and, therefore, experiences the most stress. You need two elements to correct this problem. First, replace the standard braid with a double-served wire shield. As a result of many years of testing, this shield type has proven optimal for flex life and shielding effectiveness. You must isolate the shield from the conductors and the outer jacket to reduce friction in the shield wires. This friction generates heat and reduces

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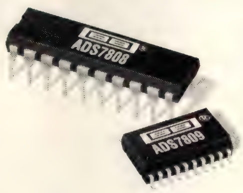

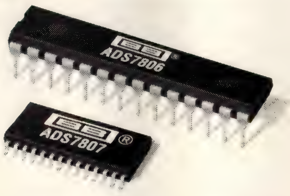

Compact, 12- & 16-Bit Serial Output A/Ds

ADS7808 and **ADS7809** are 12-bit and 16-bit, general purpose, serial output A/Ds. Both deliver 100kHz sampling rates with very low 100mW power dissipation using a single +5V supply. Ideal for many low power, portable applications requiring high sampling rates with superior accuracy and spectral purity, they're perfect for spectrum analyzers, portable oscilloscopes and vibration analyzers, medical electronics, and process control applications—where their serial output simplifies needed isolation. Available in 20-pin 0.3" plastic DIPs and SOICs. **ADS7808** is priced from **$9.95** in 100s; **ADS7809** from **$28.85.**

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12- & 16-Bit, Low Power CMOS Sampling A/Ds

ADS7806 and **ADS7807** are 12-bit and 16-bit, pin-compatible, low power A/Ds. Both sample at 40kHz and consume less than 35mW from a single +5V supply. A stand-by mode consumes only 50µW power. ADS7806 specs: 12-bits, 35mW power dissipation, ±1/2 LSB INL, "no missing codes" DNL, 72dB SINAD, and 80dB SFDR. ADS7807 specs: 16-bit resolution, 35mW power dissipation, ±3/2 LSB INL, "no missing codes" DNL, 86dB SINAD, and 90dB SFDR. Available in 28-pin 0.3" plastic DIP and SOIC, **ADS7806** is priced from **$9.85** in 100s; **ADS7807** from **$28.95**.

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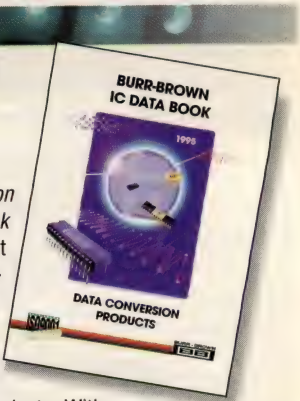

Our new *Data Conversion Products IC Data Book* contains complete product descriptions, specifications, applications tips, and ordering information for a broad line of our high performance, high quality data conversion products. With over 1200 pages, it offers more than 25 new high performance data conversion solutions. New products profiled include: A/D and D/A converters, data acquisition components, sample/hold amplifiers, V/F converters, multiplexers, and demonstration boards. The *Data Conversion Products* data book is **FREE** from any Burr-Brown sales office or representative. Or, call the Literature Hot Line at **(800) 548-6132** to get your copy.

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ADS7805

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ADS7804 and **ADS7805** are 12-bit and 16-bit A/Ds with a sample/hold, precision voltage reference, clock, microprocessor interface, and three-state output drivers on the chip. They accept ±10V inputs, require only a single +5V supply, with "no missing codes". ADS7804 specs: 12-bits, 72dB SINAD (45kHz input signal), ±0.5 LSB max INL, 100kHz min sampling rate, and 100mW max power dissipation. ADS7805 specs: 16-bits, 86dB SINAD (45kHz input signal), ±1.5 LSB max INL, 100kHz sampling rate, and 100mW max power dissipation. All are packaged in compact, 28-pin 0.3" plastic DIPs or SOICs. **ADS7804** is priced from **$22.15** in 100s; **ADS7805** from **$13.50.**

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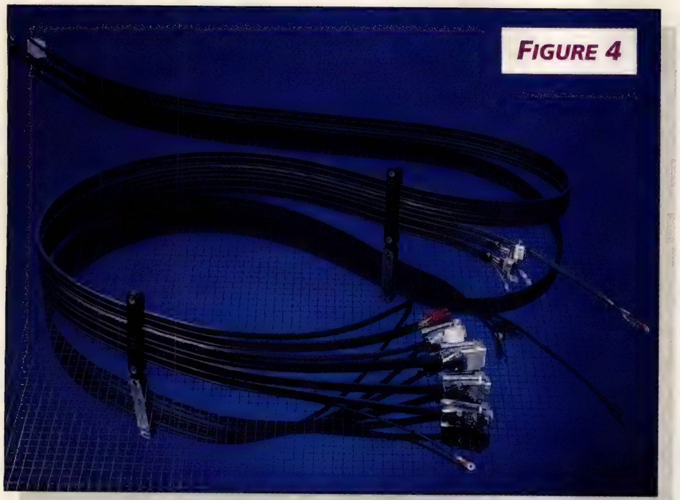


FIGURE 4

The relatively low mass of a ribbon cable improves reliability in applications with cable acceleration.

flex life. Second, you need to use material with a low coefficient of friction (both static and dynamic) to isolate the shield from the cable. Fluoropolymer-based materials, such as GORE-TEX Expanded PTFE, have the lowest coefficient of friction of any cable material. Designers have used these materials for applications ranging from coaxial dielectric to ruggedized outer jackets on limp gimbal cables.

The cable jacket protects the shield and conductors from the environment. If you properly clamp and terminate the cable, the jacket can increase the pull strength and flex life of the cable. You should keep jacket thickness to a minimum to keep the cable diameter down. Therefore, materials with high tensile strength and tear resistance are desirable. Your cable also needs resistance to hydraulic, cutting fluid, and solvents. An excellent material for cable jackets is polyurethane because it is flame-retardant, resists most industrial fluids, and has excellent abrasion resistance.

As cycle times reduce, the weight of the cable and cable-management system become limiting factors. In these applications, you can use a ribbon power cable instead of a standard power cable. The flex life of the ribbon cable is 100 times greater than the round cable (**Fig 4**). The ribbon cable is one-fourth the weight of the round cable. Ribbon cables help you reduce the mass of the moving cable bundle, allowing greater acceleration, less vibration and oscillation, and decreased wear.

You can often flex and move a ribbon cable without the use of a cable chain. The ribbon cable is self-supporting and, with the proper clamps and guides, can be used in most rolling, torsional, and tick-tock (back-and-forth) flex applications. The cable can also feature mounting brackets molded onto the jacket, which results in significant cable installation labor savings.

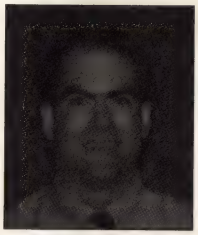
The ribbon cable offers greater flex life, lower weight, and other advantages over round cables and cable chains in flex applications. Unfortunately, you can't easily add or replace wires in ribbon cables. For this application, you can use a cable chain. New cable chains are available that are 50 to 75% lighter than existing standard cable chains. These chains have no moving parts, and you can simply snap in round or flat cables. The segments can be riveted together in any combinations of sizes. By contrast, standard cable chains have molded links that snap together. The links rub against each other, generate particles, and make noise. The molded parts have sharp edges and mold lines that can abrade cables and tubes.

Reference

Moll, Kenneth W and David R McCarter, "Flex Life in Cables," *Electronic Packaging and Production*, June 1976.

Authors' biographies

Paul Warren is a product manager at the Electronics Product Division of WL Gore & Associates, Manor, TX, where he has worked for 13 years. Warren received a BSME from the University of Texas, Austin, TX. In his spare time, he enjoys off-road motorcycling, biking, and tennis.



Tom Rosenmayer is the product development leader at the Industrial Electronics Business Group of WL Gore & Associates, Austin, TX, where he has worked for three years. Rosenmayer holds a BS in metallurgical engineering from the University of Missouri, Rolla, MO, and an MS and a PhD in materials science from Rice University, Houston. He enjoys golf and computers.

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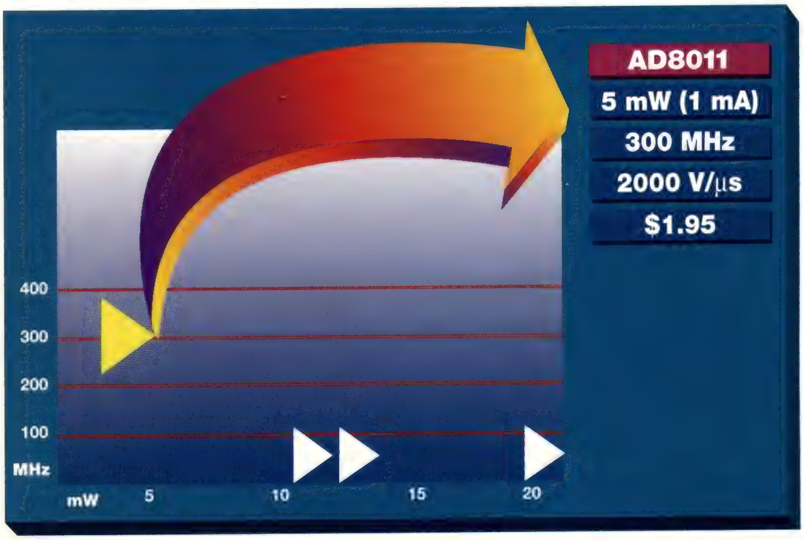


New

Fastest Amplifier with only 1 mA of Supply Current, for only $1.95

The AD8011 is the first high-speed op amp to provide all the performance you need on 1 mA, while operating on +5 V or ±5 V supplies, for a lower cost than you're paying now. Specs like these give the AD8011 the best AC performance per mA in the industry: 300 MHz bandwidth; 2000 V/μs slew rate; 29 ns to 0.1% settling time; 0.02% differential gain and 0.06° differential phase error; 0.1 dB flatness to 25 MHz; and low distortion of -70 dB at 5 MHz.

The ultralow 5 mW of power consumption and no-compromise specs make the AD8011 ideal for battery-powered systems, professional video equipment and buffering high-speed 8- to 12-bit ADCs.

AD8011 Price $1.95 Faxcode 1863 Circle 01

New

OP27 Performance with Rail-to-Rail I/O

Look to the OP284 dual op amp when you need the precision of the industry standard OP27 with rail-to-rail performance. And if you've been searching for a precision quad in a narrow 14-pin SOIC, your search has ended with the OP484.

This premier part has a maximum 65 μV offset voltage and very low 3.9 nV/√Hz noise. Combine these specifications with 4 MHz bandwidth and nearly 5 V/μs slew rate, and the unrivaled advantages of this product become obvious. In case that isn't enough, power consumption is kept low with a maximum supply current of 1.25 mA per amplifier.

PLL loop filters and battery-powered instrumentation yield unbeatable performance when the OP284 is brought into the equation.

OP284 (Dual) Price $2.93 Faxcode 1871 Circle 02
OP484 (Quad) Price $5.27 Faxcode 1871 Circle 03

KEY FEATURES
- Low offset voltage: 65 μV
- Low noise: 3.9 nV/√Hz
- +3 V to ±15 V operation

	OP284 @ +5 V	vs	OP27 @ ±15 V
V_{OS} (μV)	65		25
e_n (nV/√Hz)	3.9		3.0
GBP (MHz)	4		8
I_{SY} (mA/Amp max)	1.25		3.2

All prices shown in USD, 1000s, recommended resale, FOB USA

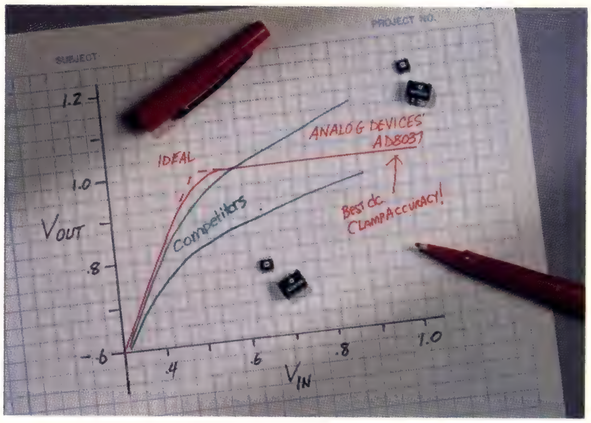
New Class of Clamped Amplifiers Improve Accuracy, Linearity

Our input-clamped, unity-gain-stable 240 MHz AD8036 and 270 MHz (G = +2) AD8037 exhibit less than ±10 mV of clamp error. Extremely fast and accurate pulse response (16 ns to 0.01% of full scale) and low distortion behavior (THD of AD8036 = -72 dBc at 20 MHz) in the unclamped region combine for driving A/D converters with protection against overdrive.

The AD8036 and AD8037 have the clamp values as additional inputs to the amplifier, and this patented architecture allows a myriad of applications such as a full wave rectifier or programmable pulse generator.

The AD9631 (unity-gain stable) and AD9632 (stable at gains of two or greater) are unclamped options to these products.

KEY FEATURES
- Clamp accuracy: 5 mV max
- Low distortion: -72 dBc @ 20 MHz
- Clamp input bandwidth up to 240 MHz



AD8036	Price $4.12	Faxcode 1836	Circle 04
AD8037	Price $4.12	Faxcode 1836	Circle 05
AD9631	Price $4.12	Faxcode 1468	Circle 06
AD9632	Price $4.12	Faxcode 1468	Circle 07

New

600 MHz, Low-Power Dual Amplifier

This 600 MHz, current-feedback amplifier is a dual version of the popular AD8001. The AD8002 delivers double the performance in the same 8-pin package, driving up to 8 video loads while maintaining good differential gain (0.01%) and phase (0.17°).

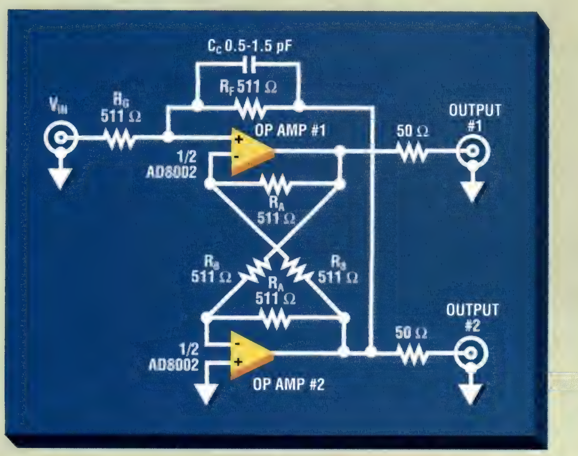
This high-performance, low-power video product is ideal for switchers, routers, distribution amplifiers, plug-in boards and CCD cameras. It is also recommended for driving differential loads such as transformers and twisted pair, where high output current is required.

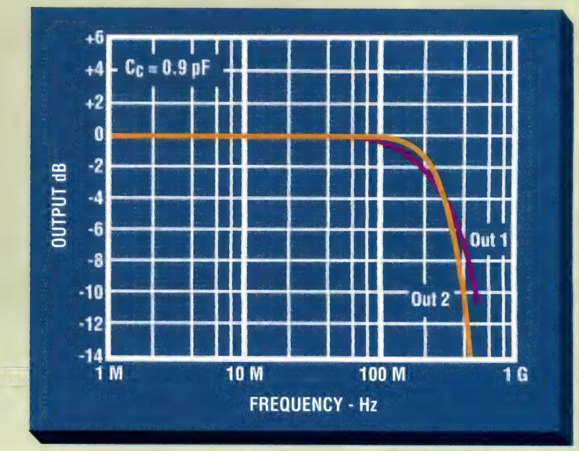
KEY FEATURES
- Low power: 5 mA/amp
- Great diff gain (0.01%) and phase (0.02°)
- Slew rate: 1200 V/µs

AD8001(Single)	Price $2.75	Faxcode 1396	Circle 08
AD8002(Dual)	Price $3.50	Faxcode 1834	Circle 09

WIDEBAND DIFFERENTIAL DRIVER

Very high-speed differential driving is often required in communications and video equipment. The two halves of the dual AD8002 can be configured to create a single-ended to differential high-speed driver with a -3 dB bandwidth in excess of 200 MHz. The AD8002 is a current-feedback amplifier, however, this overall circuit configuration yields an architecture with attributes normally associated with voltage-feedback amplifiers, while offering the speed advantages of a current-feedback amplifier. In addition, the gain of the circuit can be varied with a single resistor R_F, and unlike current-feedback amplifiers, a capacitor can be placed in the feedback path for filtering or adjusting the frequency response.





High Speed

Unbeatable Performance for the Power with Easy-to-Use Voltage Feedback Amplifiers

These amplifiers are capable of driving 50 pF capacitive loads at very low distortion. They offer superior full-power bandwidth and distortion, as well as accurate differential gain and phase of 0.01% and 0.02°. This combination of features makes the AD8047/8 ideal for driving low-power ADCs in power-sensitive video imaging and data acquisition systems, in addition to active filters, IF/RF amplifiers, or cable drivers.

For the power, these are the premier performance voltage-feedback amplifiers available today. The AD8047 is unity-gain stable, while the AD8048 is stable at gains of two or greater.

KEY FEATURES:
- 250 MHz bandwidth
- High slew rate: 750 V/µs
- Low supply current: 5.8 mA

AD8047	Price $2.33	Faxcode 1868	Circle 10
AD8048	Price $2.33	Faxcode 1868	Circle 11

High Speed, Single Supply

New

Quad, 150 MHz, 3500 V/µs Amplifier

The unique AD8004 is a four-channel, current-feedback amplifier with a slew rate of 3500 V/µs. The AD8004 operates on single or dual supplies (+5 V or ±5 V) with a low supply current of 3.5 mA per amplifier. The product is capable of delivering up to 50 mA of load current.

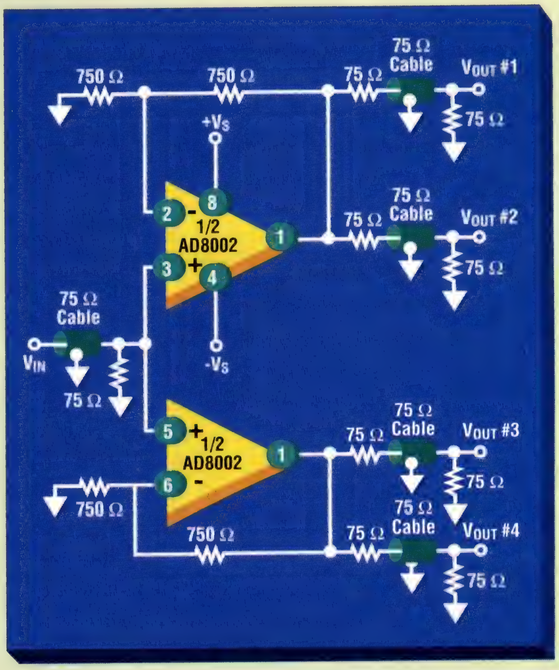
The AD8004 – the only high-speed, single-supply quad – not only has exceptionally low power, but great video specifications as well.

KEY FEATURES
- 150 MHz bandwidth; 3500 V/µs slew rate
- 3.5 mA/amp max
- Operates on single +5 V or dual ±5 V supplies

AD8004	Price $5.95	Faxcode 1835	Circle 12

DRIVING MULTIPLE VIDEO LOADS

The dual AD8002 has been designed to offer outstanding performance as a video line driver. The critical specifications of differential gain (0.01%) and differential phase (0.02°) meet the most exacting HDTV demands for driving one video load with each amplifier. The AD8002 also drives four back-terminated loads (two each), with equally impressive performance (0.01%, 0.07°). In fact, the AD8002 is capable of driving eight 75 Ω back-terminated loads (four each) while maintaining 0.01% differential gain and 0.17° differential phase performance.



New

Fastest Rail-to-Rail FET Amplifier

This 16 MHz dual op amp operates from +3 V to +36 V with exceptional rail-to-rail output performance. The input voltage range extends below ground when operating single supply. The AD823 has input bias currents below 25 pA and a low offset voltage of 800 µV.

The combination of AC and DC performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for applications such as A/D drivers, high-speed active filters, and other low-voltage, high dynamic range systems.

KEY FEATURES

- 16 MHz bandwidth
- Ib = 25 pA max
- Capacitive load drive: 500 pF

AD823 Price $2.25 Faxcode 1907 Circle 13

Excellent Video Performance with +3 V to ±15 V Operation

The AD812 is a dual amplifier offering excellent video specifications of .1 dB flatness to 40 MHz and differential gain and phase error of 0.02% and 0.02°. The combination of high performance, +3 V operation and low cost SO-8 packaging makes the AD812 dual suitable for applications requiring multiple amplifiers.

The AD812 has fast slew rate and settling time (50 ns to 0.1%). It also offers low distortion and low noise of 3.5 nV/√Hz, making it suitable for a variety of applications. You will find the AD812 ideal for applications such as portable cameras, video switchers and video line drivers.

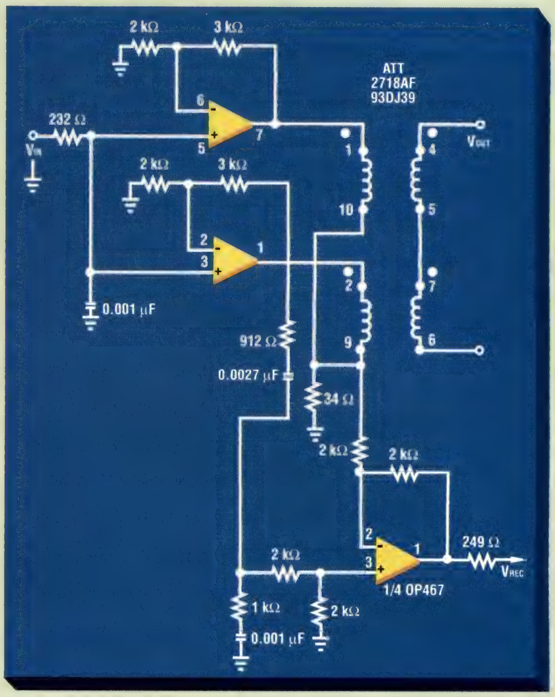
KEY FEATURES

- 145 MHz; 1600 V/µs
- High output drive: 50 mA
- +3 V to ±15 V operation

AD812 Price $2.48 Faxcode 1402 Circle 14

TWISTED PAIR DRIVER

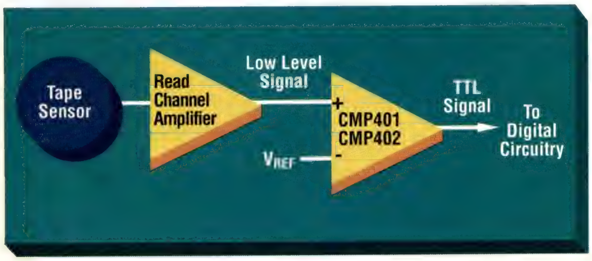
HDSL (High-bit-rate Digital Subscriber Line) uses twisted copper to support voice and data information primarily for business-to-business communications. Although the output drive requirements are not as stringent as some applications, HDSL requires operation on low ±5 V supplies. Therefore, the driving amplifier must be able to provide a large output swing and deliver high-output current close to the rails. As shown in the accompanying diagram, the AD812 dual amplifier can provide the required output swing and current on ±5 V supplies. The power is summed via a parallel connection of primaries of the transformer coupled to a series connection of the secondaries of the transformer. The quad, low-noise OP467 is used as the receiver. Additionally, the AD8042 can be used as the drive amplifier if a single +5 V supply is required.



New

Fastest +3 V Comparator Handles ±5 V Inputs

Detect high speed signals and interface to three- or five-volt logic with ADI's new quad comparator – the CMP401. Its 20 ns propagation delay and wide input range make it ideal for data detection in magnetic or optical memories and for line receivers. Total supply current is only 7 mA, greatly reducing power over other high-speed comparators.



And for even lower power, choose the CMP402 which requires only half the power. The CMP402 propagation delay is 40 ns. Separate input supplies can handle +3 V to ±5 V and outputs can be powered from either +3 V or +5 V.

KEY FEATURES
- Propagation delay only 20 ns
- Supply range: +3 V to ±5 V
- Separate analog and digital supplies

CMP401	Price $3.90	Faxcode 1872	Circle 15
CMP402	Price $3.90	Faxcode 1872	Circle 16

New

160 MHz Rail-to-Rail Amplifier with Disable, $1.50

This low-power, voltage-feedback amplifier is fully specified for +3, +5, and ±5 V supplies. The input voltage range extends below the negative rail, allowing the AD8041 to accommodate input signals below ground when operating from a single supply. The product has gain flatness of 0.1 dB to 30 MHz while offering differential gain and phase error of only 0.02% and 0.03° on a +5 V supply.

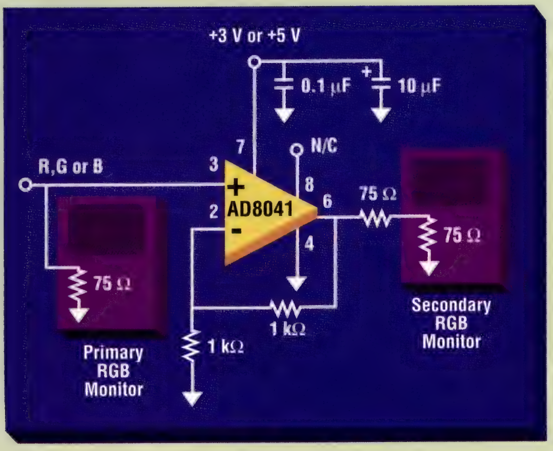
The AD8041 also has a high-speed disable feature and a low supply current of 5.8 mA max. For the price, you can't beat the performance. Dual and quad versions of this exciting amplifier will be available soon.

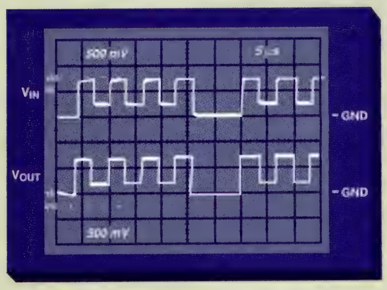
KEY FEATURES
- Wide supply range: +3 V to ±5 V
- 160 MHz bandwidth
- Sources and sinks 50 mA to within 0.5 V of supply rails

AD8041(Single)	Price $1.50	Faxcode 1925	Circle 17
AD8042(Dual)	Price $2.25	Faxcode 1929	Circle 18

SINGLE-SUPPLY RGB AMPLIFIER

The AD8041 can provide buffering of RGB signals that include ground while operating from a single +3 V or +5 V supply. The signals that drive an RGB monitor are usually supplied by current-output DACs that operate from a +5 V supply. These can be triple DACs like the ADV7120 and ADV7122 from Analog Devices or DACs integrated into the graphics controller IC as in most PCs.





Since the RGB signals include ground as part of their dynamic output range, a dual-supply op amp has previously been required to provide this buffering. In some systems this is the only component that requires a negative supply, so it can be quite inconvenient to incorporate the buffer.

Shown above is an oscilloscope photo of the AD8041 operating from a +3 V supply and driven by the blue signal of a color bar pattern. Note that the input and output are at ground during the horizontal blanking interval.

Rugged 3 MHz GBP Amplifier Requires Only 350 µA and has Rail-to-Rail Inputs and Outputs

Whether your application is automotive, computer or portable instrumentation, the OP191 family offers the performance you'll need to make your design a success. Offset voltage is below 700 µV and the rail-to-rail output can supply ±8 mA.

The OP191 is a rugged amplifier. Inputs are uniquely protected against overvoltage and can handle up to 5 V beyond either supply. It is guaranteed over the -40 to +125° C temperature range and is fully specified at +3 V, +5 V and ±5 V.

KEY FEATURES

- Operation from 2.7 V to 12 V
- 3 MHz GBP
- Slew rate: 0.5 V/µs

OP191(Single)	Price $1.34	Faxcode 1809	Circle 19
OP291(Dual)	Price $1.68	Faxcode 1809	Circle 20
OP491(Quad)	Price $2.76	Faxcode 1809	Circle 21

Rail-to-Rail JFET Operates from +3 V to +30 V

When your design can tolerate only picoamps of input current and you need precision rail-to-rail performance, there is only one solution – the AD820. (And, of course, our dual AD822 and quad AD824.) The AD820 is trimmed for both temperature drift and offset, making the drift comparable to that of high-performance bipolar amplifiers. Single-supply operation from +3 to +30 V and reduced drift make this a unique FET amplifier.

This exceptional performance combined with 16 nV/√Hz noise and 620 µA supply current make the AD820 the perfect choice for medical systems and instruments. The combination of low noise, low power, and small package size allow for increased board density – yielding smaller, more power-efficient systems.

KEY FEATURES

- Input bias current: 2 pA
- Voltage noise density: 16 nV/√Hz
- AD824 quad in narrow SO-14 package

AD820(Single)	Price $1.28	Faxcode 1406	Circle 22
AD822(Dual)	Price $2.04	Faxcode 1407	Circle 23
AD824(Quad)	Price $3.38	Faxcode 1810	Circle 24

RAIL-TO-RAIL AMPLIFIER SELECTION GUIDE

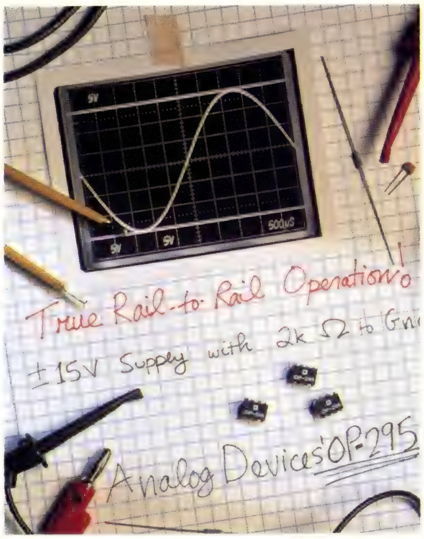
	Part Number			Supply Voltage				Rail-to-Rail		Vos	Slew	e Noise	I Out	I Sup	GBP	
	Single	Dual	Quad	3 V	5 V	12 V	±15 V	In	Out	(µV)	(V/µs)	(nV/√Hz)	(mA)	(mA)	(MHz)	Key Feature
OP		284	484	•	•	•	•	•	•	65	2.4	3.9	±8	1.25	4	OP27 performance with SS
OP	191	291	491	•	•	•		•	•	500	0.4	35	±13	0.35	3	Low power R-R I/O
OP		296	496	•	•	•		•	•	500	0.1	35	±2	0.05	0.3	Micropower R-R I/O
OP		295	495	•	•	•	•		•	300	0.03	51	±18	0.15	0.075	Accuracy and output drive
AD	820	822	824	•	•	•	•		•	400	3	16	±25	0.5	2	JFET input, low power
AD		823		•	•	•	•		•	800	22	16	±15	2.6	16	Fast JFET input
AD	8041	8042		•	•	•		•	•	3000	150	16	±50	5	160	Fastest R-R video
OP		279			•	•		•	•	4000	3	22	±80	3.5	5	80 mA output current

+3 V to +30 V Precision Rail-to-Rail Op Amp

When you need more signal range and drive from your design's ASIC or DAC, the OP295 delivers rail-to-rail performance with high output current. Use the wide output swing to dramatically increase the adjustment range of tuning circuits that tap DAC output values. Or take advantage of the OP295's ±18 mA to give ASICs the power to drive loads ranging from coax cables to power transistors.

Excellent dc characteristics make the OP295 the ideal choice to add drive to high accuracy systems operating from +3 V to ±15 V. And in the low-voltage range of portable and battery-powered applications, the 150 µA supply current makes the dual OP295 and the quad OP495 indispensable.

KEY FEATURES
- Low offset voltage: 300 µV
- Rail-to-rail output swing
- Low supply current: 150 µA



OP295(Dual)	Price $1.98	Faxcode 1698	Circle 25
OP495(Quad)	Price $3.56	Faxcode 1698	Circle 26

New Few Amplifiers Hint at +2 V Operation, the OP193 Family Guarantees It

When your design requires high precision at the lowest possible power, select one of the OP193 family of amplifiers. These low-power amplifiers combine low supply current and guaranteed operation at +2 volts to make your product deliver higher performance and run longer than your competitor's.

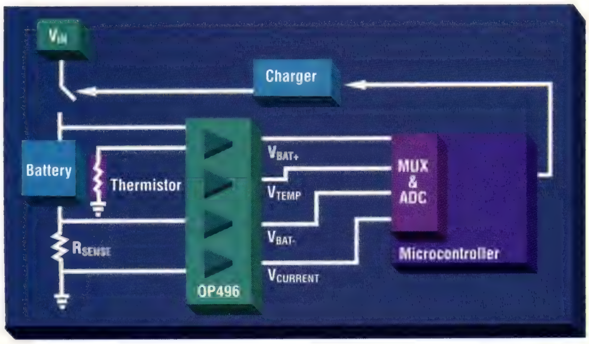
The OP193 family's performance is ideal for industrial designs. Offset voltage is 75 µV, and low drift and high CMRR help maintain this excellent accuracy. Operation is fully specified and guaranteed from single supplies as low as 2.0 V and dual supplies up to ±15 V. Supply current is only 25 µA per amplifier and outputs sink and source current.

KEY FEATURES
- Low offset voltage: 75 µV
- Low supply current: 25 µA/amp max
- Standard dual SO-8 pinout

OP193(Single)	Price $1.37	Faxcode 1856	Circle 27
OP293(Dual)	Price $2.07	Faxcode 1856	Circle 28
OP493(Quad)	Price $2.73	Faxcode 1856	Circle 29

New 45 µA Precision Rail-to-Rail Op Amp

Do you need to monitor your battery without draining it? Would you like to resolve small input signals and maintain a wide signal range? It's never been this simple. The OP496 makes battery monitoring easy while leaving the power in your battery. Rail-to-rail inputs and outputs are essential for low-voltage applications and the OP496 provides both.



Not only is power consumption low, but this quad amplifier offers 300 kHz of bandwidth with only 45 µA supply current. Precision and performance make the OP496 useful in a wide variety of applications, such as: sensor interfaces, system monitors for power-off conditions, and security systems.

KEY FEATURES:
- Low power: 45 µA/amp max
- Rail-to-rail inputs and outputs
- Gain bandwidth: 300 kHz

OP296(Dual)	Price $1.37	Faxcode 1926	Circle 30
OP496(Quad)	Price $2.10	Faxcode 1926	Circle 31

Single Supply, Low Noise

+5 V Audio Pair

The SSM2135 and the OP279 are an ideal pair for handling audio inputs and outputs in 5 V systems. For inputs, choose the SSM2135. It features low noise density and distortion below 0.003%. Output stages benefit from the OP279's rail-to-rail inputs and its high-current, rail-to-rail outputs.

The OP279's 80 mA output current easily drives headphones – even with 32 Ω impedance – and the 5 MHz bandwidth and 3 V/µs slew rate keep distortion low. OP279s are often used to buffer audio DACs or ASICs that have wide output swings but limited drive capability.

Low-noise, high-gain input stages require all the performance of the SSM2135. With its low 5.2 nV/√Hz input noise and 3.5 MHz bandwidth, you can design 5 V computer audio systems that approach professional-quality audio.

SSM2135	Price $1.78	Faxcode 1794	Circle 32
OP279	Price $1.18	Faxcode 1811	Circle 33

Low-Noise, Low-Drift Amplifier

Select the OP113 to maintain your system's accuracy with guaranteed offset drift of 0.8 µV/° C and low noise density of 4.7 nV√Hz. The combination of low offset voltage, high gain, and high CMRR yields excellent precision in both single- and dual-supply designs.

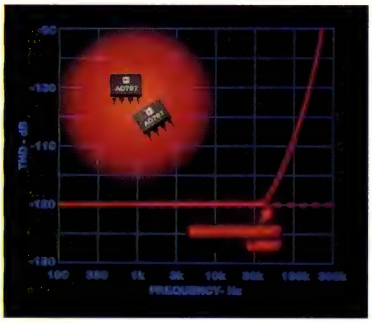
The extremely wide dynamic range required by industrial systems, digital scales, and strain gages is easily achieved with the OP113. For systems that must drive high output currents, the OP113 can deliver ±30 mA, even at 5 V. Its ability to operate at +5 V, +12 V, or ±15 V allows you to use the OP113 in a wide variety of sockets, limiting inventory requirements. Dual and quad versions – the OP213 and OP413, respectively – are also available. Pricing is another attractive feature, starting at just $1.47.

KEY FEATURES
- Low drift: 0.8 µV/° C max
- Low noise: 4.7 nV/√Hz
- High output drive: ±30 mA

OP113 (Single)	Price $1.47	Faxcode 1666	Circle 34
OP213 (Dual)	Price $1.71	Faxcode 1666	Circle 35
OP413 (Quad)	Price $3.20	Faxcode 1666	Circle 36

Low Noise

True 16-Bit Performance



Don't risk having your system's 16-bit performance degraded by noise and high offsets. Check the specs on the AD797 and find true 16-bit performance with ultralow noise and distortion. If that's not enough to get your attention, the 110 MHz GBP will.

Take advantage of the AD797's incredibly low offset voltage to obtain high accuracy in precision voltmeters. Its wide bandwidth, low noise and THD make it an excellent choice for distortion analyzers and professional audio gear.

Use the wide output swing to buffer the inputs to professional audio preamplifiers and the outputs of high resolution DACs. And don't be concerned with noise – its 0.9 nV/√Hz is the lowest in the industry.

KEY FEATURES:
- Ultralow offset voltage: 40 µV max
- Ultralow noise: 0.9 nV/√Hz @ 1 kHz
- 800 ns settling time to 16 bits

AD797	Price $3.36	Faxcode 1394	Circle 37

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ANALOG DEVICES
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A distributed arithmetic approach to designing scalable DSP chips

BERNIE NEW, XILINX INC

You can use distributed arithmetic to design DSP chips. Using look-up tables, it lets you develop hardware implementations of DSP algorithms in FPGAs. Pipelining lets you trade off speed vs logic resources.

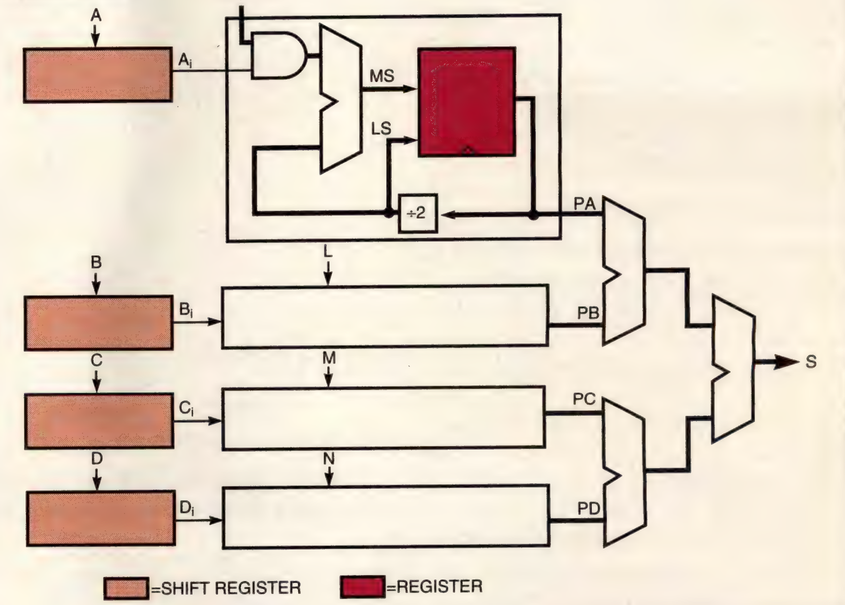
At the heart of most DSP algorithms is a multiply-and-accumulate (MAC) function that you can implement more efficiently with distributed-arithmetic techniques than by using conventional arithmetic methods. Distributed arithmetic makes extensive use of look-up tables (LUTs), which makes it ideal for implementing DSP functions in LUT-based field-programmable gate arrays (FPGAs).

An additional advantage is an easy trade-off between output sample rate and resource utilization. You can use a minimum set of LUTs and adders in a sequential implementation to minimize cost. For higher speed, you replicate the set of LUTs and include more adders. You can vary the number of LUTs used to achieve the desired speed. If enough LUTs are available to process all the incoming data bits simultaneously, the chip can perform MAC operations at the full clock rate.

Distributed arithmetic

Distributed arithmetic differs from conventional arithmetic only in the order in which it performs operations. As an example, **Fig 1** is a conventional four-product MAC that uses a sequential shift-and-add technique to multiply four pairs of numbers and sum the results. Each multiplier forms partial products by multiplying the coefficient by 1 bit of data at a time in an AND function. The technique then adds these partial products into an accumulator that shifts 1 bit position each clock cycle,

FIGURE 1



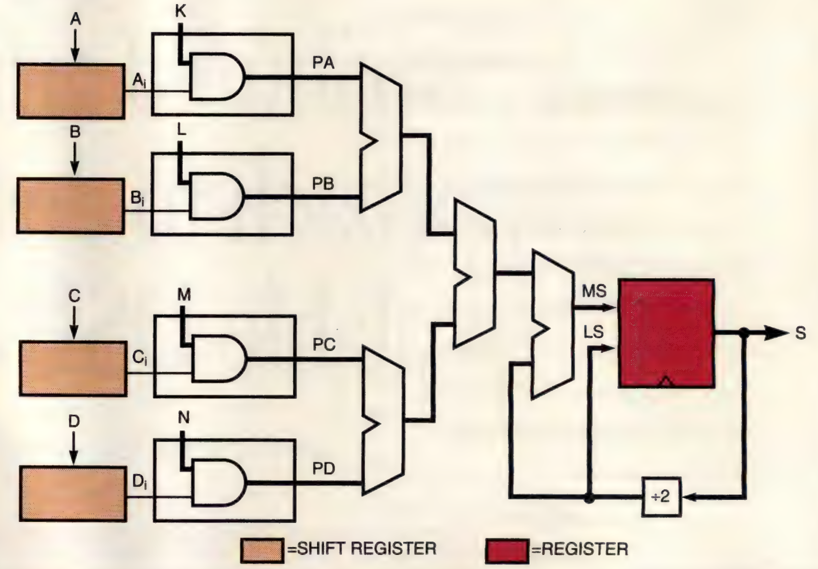
A conventional four-product MAC uses a sequential shift-and-add technique to multiply number pairs and sum the result.

thus appropriately weighting the partial products. The arithmetic then simultaneously performs four multiplications and sums the results when the products are complete. During each clock cycle, the four multipliers create four partial products, all with the same weight, which eventually sum into the output. Distributed arithmetic adds the partial products before, rather than after, weighing and accumulating them.

Fig 2 shows the same MAC, which reorders the operations through the use of distributed arithmetic. The technique reduces the number of shift-and-add circuits to one, but does not change the number of simple adders.

The coefficients in many DSP applications are constants. Consequently, the output of the AND functions and first three adders of **Fig 2** depends only on the 4 input bits from the shift registers. Replacing these AND functions and adders with a simple 16-word LUT gives you the final form of a distributed-arithmetic MAC (**Fig 3**).

FIGURE 2

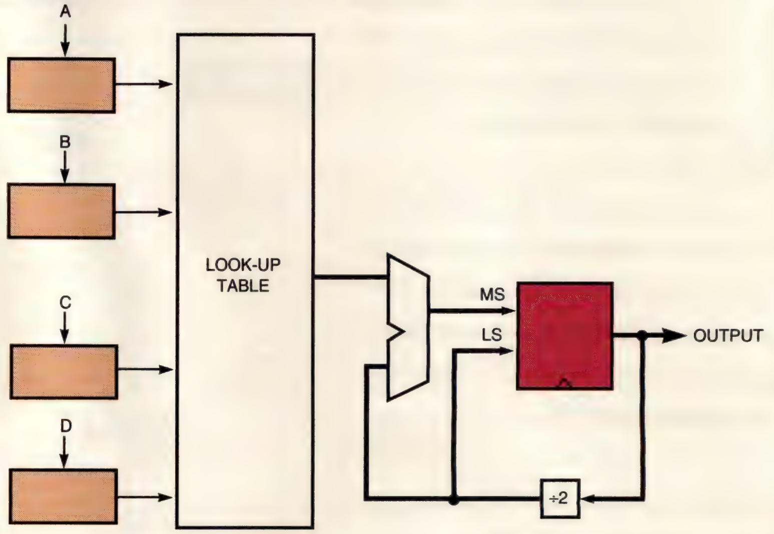


Using distributed arithmetic, this MAC adds, weights, and accumulates the coefficients.

LUT definition

The LUT data comprise various sums of the four coefficients. If the 4 data bits that address the LUT are all 1, the output is the sum of all four coefficients. Any data bit that is a 0 eliminates the corresponding coefficient from the sum. Because the address contains all possible combinations of 1 and 0 inputs, the LUT contains all possible sums of the coefficients (**Table 1**).

FIGURE 3



A look-up table (LUT) of an appropriate size replaces the AND gates and three adders of a distributed-arithmetic MAC.

In the four-coefficient example, the width of the LUT is typically 2 bits greater than the coefficient width. The additional 2 bits allow for word growth from the addition of the coefficients. The circuit requires at most 2 bits because the circuit is summing no more than four coefficients. Fewer additional bits may be adequate in cases in which the combinations of coefficients result in less word growth. More than four coefficients require more space for word growth. In general, the number of additional bits should be at least $\log_2$ (number of coefficients). You can use fewer bits only when you have determined the coefficients and computed the LUT contents to fit into a narrower word.

As the number of coefficients increases, the size of the LUT grows exponentially. You can avoid the problem of large LUTs by partitioning the multiplications into smaller groups and combining the LUT outputs with adders. The adders are less costly than the larger LUT. For example, if an FPGA uses 16-bit LUTs as four-input function generators, the optimum partition is four products per LUT. You can partition a 16-

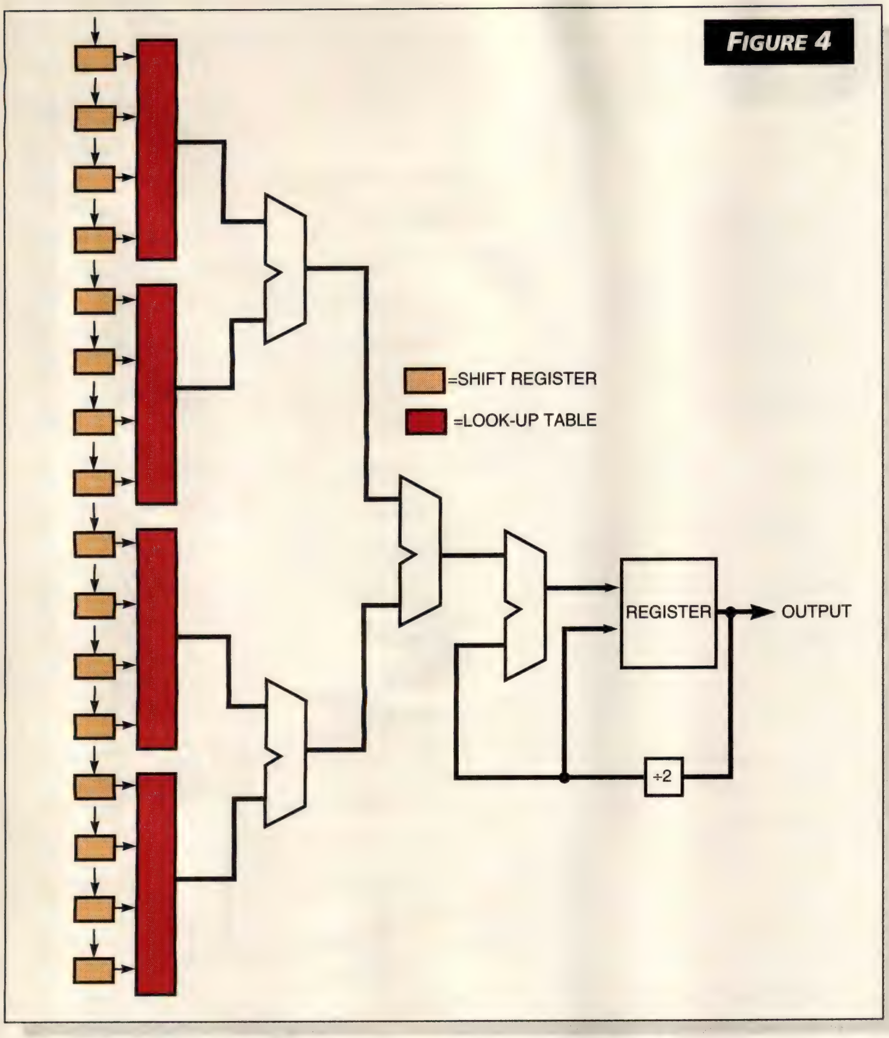


FIGURE 4
=SHIFT REGISTER
=LOOK-UP TABLE
REGISTER
OUTPUT
÷2

You can partition a 16-input distributed-arithmetic MAC with four products per 16-bit LUT. Because the size of the LUT grows exponentially with the number of coefficients, this is an efficient way of handling larger numbers of inputs.

product MAC in this way (**Fig 4**). Instead of increasing the LUT size by a factor of 16, four LUTs are the same size as the one used in the four-product MAC of **Fig 3**. Using built-in carry logic, the adders are approximately the same size as the LUTs, and the total growth is a factor of only seven. You can program the small LUTs in the same way as in the four-product MAC.

FIR filters and MACs differ only in how they handle the input data (**Fig 5**). The MAC has a series of parallel-to-serial converters, but the filter has one long, bitwide shift register that taps into every word and parallel-loads only in its first word. The shift register operates by parallel-loading the new data sample into the first word of the shift register. The shift register then shifts all the data until they move 1 word, presenting each word, 1 bit at a time, to the LUTs. When the shifting is complete, the first word is empty and is ready to again parallel-load. The data already in the shift register position for the appropriate coefficient to multiply the data in the next filter cycle and lose the oldest data word. You can construct such a shift register using flip-flops. A more efficient implementation, however, uses RAM for all words except the first.

In addition to providing ROM LUTs, you can configure the function generators in SRAM-based FPGAs as 16-bit

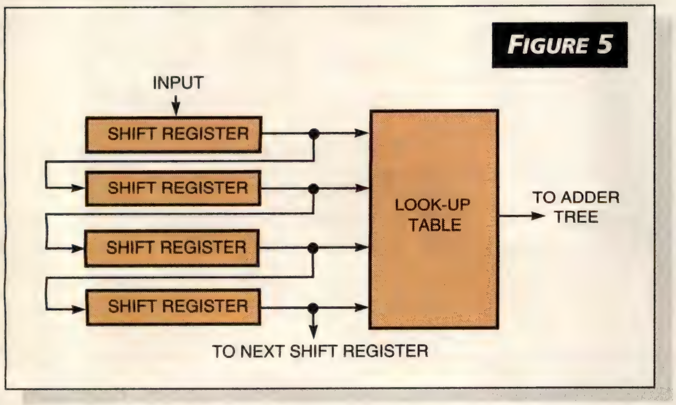


FIGURE 5
INPUT
SHIFT REGISTER
SHIFT REGISTER
SHIFT REGISTER
SHIFT REGISTER
LOOK-UP TABLE
TO ADDER TREE
TO NEXT SHIFT REGISTER

Modifying a MAC allows it to be used as a distributed-arithmetic FIR filter. The filter has one long bit-wide shift register that is tapped every word and can be parallel-loaded only in the first word.

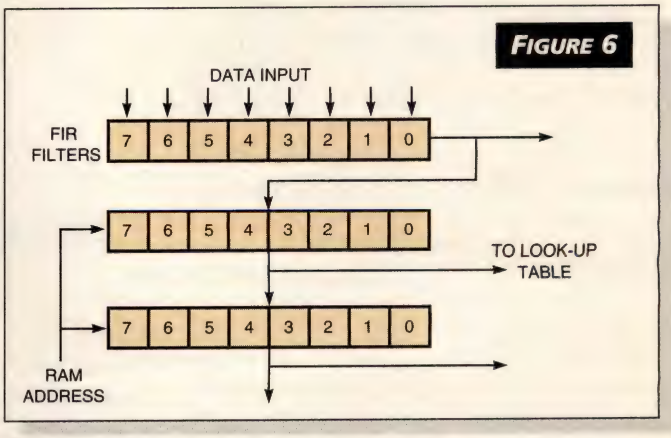


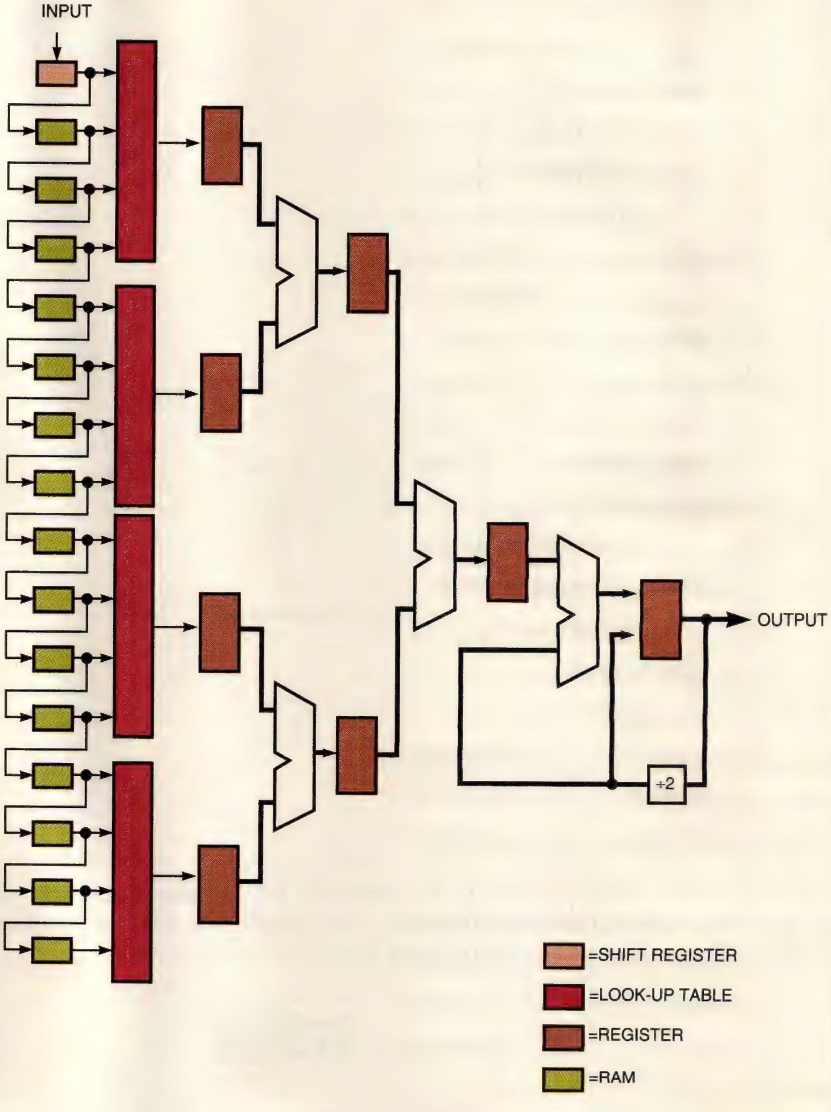
FIGURE 6
DATA INPUT
FIR FILTERS
7 6 5 4 3 2 1 0
7 6 5 4 3 2 1 0
7 6 5 4 3 2 1 0
TO LOOK-UP TABLE
RAM ADDRESS

A more efficient way to implement a distributed-arithmetic FIR filter is to replace the shift registers with RAM for all but the first word.

RAMs, which suit the data-storage needs of digital filters. The following example uses a read-modify-write technique for a distributed-arithmetic FIR filter. The example uses Xilinx's XC4000 FPGA family. Individual 1-bit-wide RAMs each hold the 3 bits of a data word at successive addresses (**Fig 6**). As each bit is read and presented to the LUT, it is rewritten to the same address but in the adjacent RAM. As the multiplication continues, the data simultaneously transfer to the next RAM.

You have to implement only the first data word with flip-flops because of the need to parallel-load new data. As the first word shifts into the multiplier, the multiplier provides the input to the first RAM. All the RAMs operate synchronously and can share an address counter. This approach leads to the FIR filter design shown in **Fig 7**.

FIGURE 7



You can build a distributed-arithmetic FIR filter using flip-flops for the first data word and RAM for the rest of the words. All of the RAMs can share an address counter.

Size and performance

Each 8×1-bit RAM that stores input data uses one-half of a configurable-logic block (CLB) in the XC4000 family. A single 3-bit counter, requiring 1.5 CLBs, addresses all of the RAMs. The parallel-to-serial converter for the newest data word uses four CLBs. You can implement the complete data storage using only 14 CLBs.

The maximum value that an LUT must store is the sum of four coefficients. Consequently, the width of the LUT is at most 2 bits greater than the coefficient width. With 8-bit coefficients and four inputs per LUT, each LUT uses five CLBs. The 16-coefficient filter, thus, uses 20 CLBs to implement the LUTs.

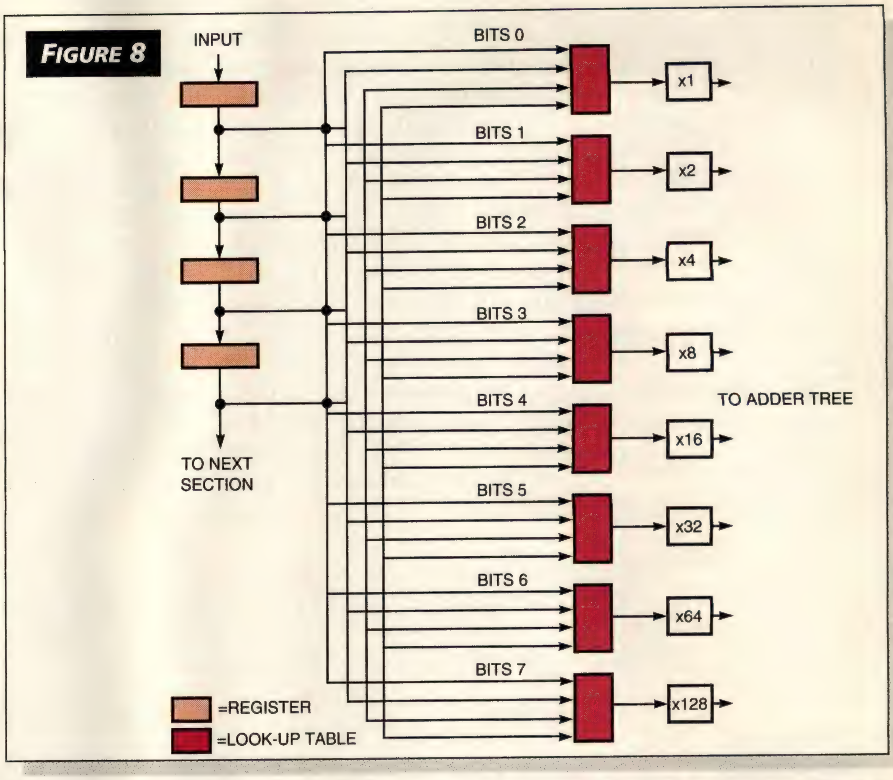
To maintain full arithmetic precision through the filter, the first adder stage that combines the LUT outputs must handle 11 bits, and the second adder stage must handle 12 bits. You can implement all three adders with 21 CLBs. The final accumulator must be able to hold as many as 20 bits; this task requires 10 CLBs. The overall CLB requirement is, at most, 65 CLBs. You may need fewer if some coefficients have low values or if the summation truncates or rounds some data. Even with the maximum CLB count of 65, you can implement the entire filter in two-thirds of an XC4003, the second smallest device in the XC4000 family, with its 10×10 array of CLBs. The same filter takes less than 7% of an XC4025, the largest family member, with its 32×32 CLB array.

Using the CLB's flip-flops, you can pipeline the filter at every stage at no additional cost. If you pipeline with the flip-flops, the speed-determining factor is the widest adder, which is in the final accumulator. The active width of this adder is only 13 bits, thanks to the sequential LSB-first operation. Consequently, you can clock the filter at approximately 40 MHz when you use the XC4000 FPGA family. With eight clock cycles for each data sample, the maximum data rate through the filter is approximately 5 MHz.

The previously described design is the slow-speed/low-cost endpoint in a speed/cost continuum. Storage cost is at its lowest because both data and coefficient stores are at their minimum. Conceivably, you could multiplex the LUTs into a smaller adder tree. With the XC4000 family, however, additional multiplexers are no smaller than the adders they replace. You would be sacrificing performance for little or no saving of FPGA logic resources.

You can improve performance by implementing additional logic on the FPGA. Generating a filter output sample accesses each LUT as many times as there are bits in the data word. Consequently, both the adder-determined clock period and the data-determined number of clocks per output sample limit the throughput.

FIGURE 8



In a parallel version of the FIR filter, each of the four LUTs in the circuit of Fig 4 is replicated eight times. The filter can now simultaneously handle all data bits, increasing throughput by a factor of eight.

Simply duplicating the LUTs so that they can simultaneously handle 2 data bits halves the clock-cycle requirement and doubles the throughput. You must correspondingly increase the size of the adder tree, but this increase significantly affects only the filter latency, not the clock period. You can obtain even higher throughput by further replicating the LUTs. Ultimately, you can replicate the LUTs as many times as there are bits in the input data. When you reach this point, all the necessary LUT accesses occur simultaneously, and every clock cycle can produce a filter output. This technique yields a fully parallel distributed-arithmetic filter.

Fig 8 shows part of the parallel version of the FIR filter. The version replicates each of the four LUTs in the sequential design eight times and weights the outputs according to the weight of the input bits. This version of the filter can simultaneously handle all of the data bits. To implement the circuit, you need 160 CLBs, five each for the 32 LUTs. The adder tree that combines the 32 LUT outputs comprises 31 adders. The adders vary in size from 11 bits in the first stage to 16 bits in the final stage. The tree provides a full 20-bit output, but a 16-bit adder is adequate because the 4 LSBs do not participate in the final addition. You can implement all 31 adders in a little more than 200 CLBs. To maximize performance, the flip-flops in these CLBs provide interstage pipelining at no additional expense.

You must also use flip-flops for the input data store. RAM

TABLE 1—CONTENTS OF A 16-WORD LOOK-UP TABLE

LUT input				LUT contents
A_i	B_i	C_i	D_i	0
0	0	0	0	0
1	0	0	0	A
0	1	0	0	B
1	1	0	0	A+B
0	0	1	0	C
1	0	1	0	A+C
0	1	1	0	B+C
1	1	1	0	A+B+C
0	0	0	1	D
1	0	0	1	A+D
0	1	0	1	B+D
1	1	0	1	A+B+D
0	0	1	1	C+D
1	0	1	1	A+C+D
0	1	1	1	B+C+D
1	1	1	1	A+B+C+D

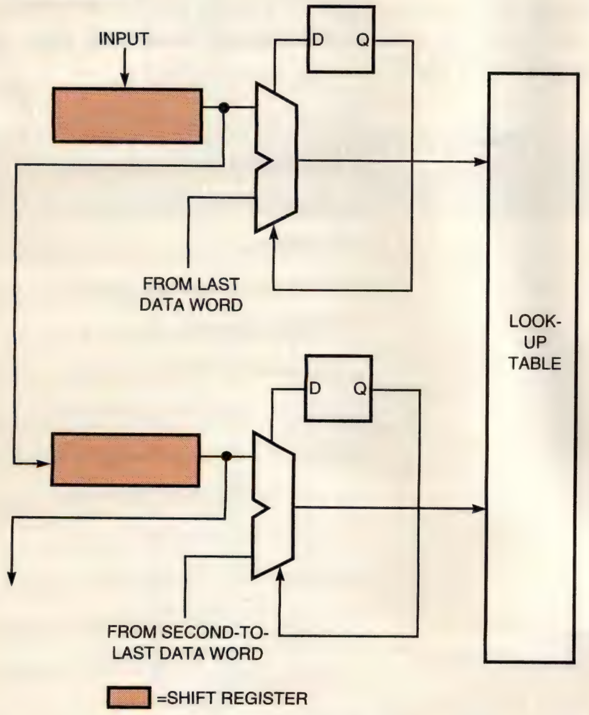
storage is inappropriate because all 128 data bits must be available simultaneously. This store is organized as a 16-word, 8-bit parallel-shift register and uses both available flip-flops in each of 64 CLBs. This store does not use the logic resources in these CLBs, which remain available for other purposes. The store requires approximately 430 CLBs, or 75% of the 24×24 CLB array in the XC4013 FPGA. You can operate the filter at clock frequencies up to 40 MHz, which the settling time of the final 16-bit adder determines. The latency is seven clock cycles with one clock per sample, and 40 MHz is also the maximum sample rate.

This example demonstrates the speed/cost scalability of the distributed-arithmetic technique. Between the sequential design and the fully parallel design is an eightfold performance increase for a sevenfold increase in CLB count. In between, opportunities exist to increase performance by a factor of two or four, with corresponding increases in logic requirements.

The distributed-arithmetic technique is not limited to basic FIR filters; you can also implement the following other common types of filters:

Linear-phase FIR filters: Linear-phase delay is synonymous with constant-time delay, a highly desirable filter characteristic. These filters delay all frequency components of the signal for the same length of time and do not change their phase relationships. Other than the attenuation of some frequencies, the output signal is simply a delayed replica of the input. This filter avoids the dramatic distortion of the waveform that can result if you allow nonlinear phase delay to disturb the phase relationships.

FIGURE 9



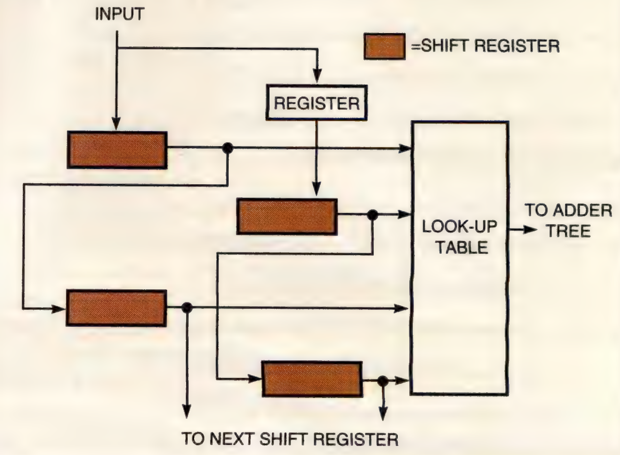
For a linear-phase FIR filter, you can place 1-bit adders before the LUT. This reduces the number of multipliers, resulting in a net decrease of required LUTs and subsequent logic resource savings.

Only FIR filters can provide an ideal *linear-phase* response and, surprisingly, linear-phase FIR filters are easier to implement than are general FIR filters. The phase response is linear only if the filter coefficients are symmetrical. The first and last coefficients must be equal, the second and the second-to-last must also be equal, and so on. You can add data words that are to be multiplied by equal coefficients before they are multiplied, thus reducing the required number of multiplications. Sequential distributed-arithmetic implementations halve the number of LUTs and correspondingly reduce the size of the adder tree. Because new premultiplication adders operate on serial-data streams, you can use simple 1-bit carry-save adders (**Fig 9**). These 1-bit adders are inexpensive and require only one CLB each, resulting in a net saving of CLBs.

Decimating FIR filters: Another unique ability of FIR filters is simple, easily implemented decimation. "Decimation" refers to limiting the signal bandwidth of a filter, which reduces the sample rate. Rather than calculating all the output samples and then discarding the unwanted ones, a FIR filter permits only the needed ones to be computed. This simplification greatly reduces the arithmetic bandwidth and is possible because each output is an independent calculation, depending only on input data.

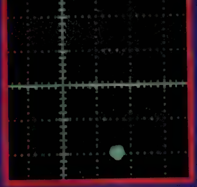
Fig 10 shows how you get decimation by a factor of two

FIGURE 10



A factor-of-two decimating FIR filter requires you to enter alternate input samples into separate shift registers.

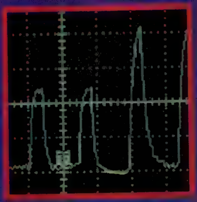
When you're trying to view a single shot event, especially near the top of the bandwidth, does it look like THIS?



UNREAL WAVEFORM:

One Point Captured. Single-event capture using Equivalent-Time sampling on a 20 MS/s, 100 MHz DSO.

When you know it really looks like THIS?



REAL WAVEFORM:

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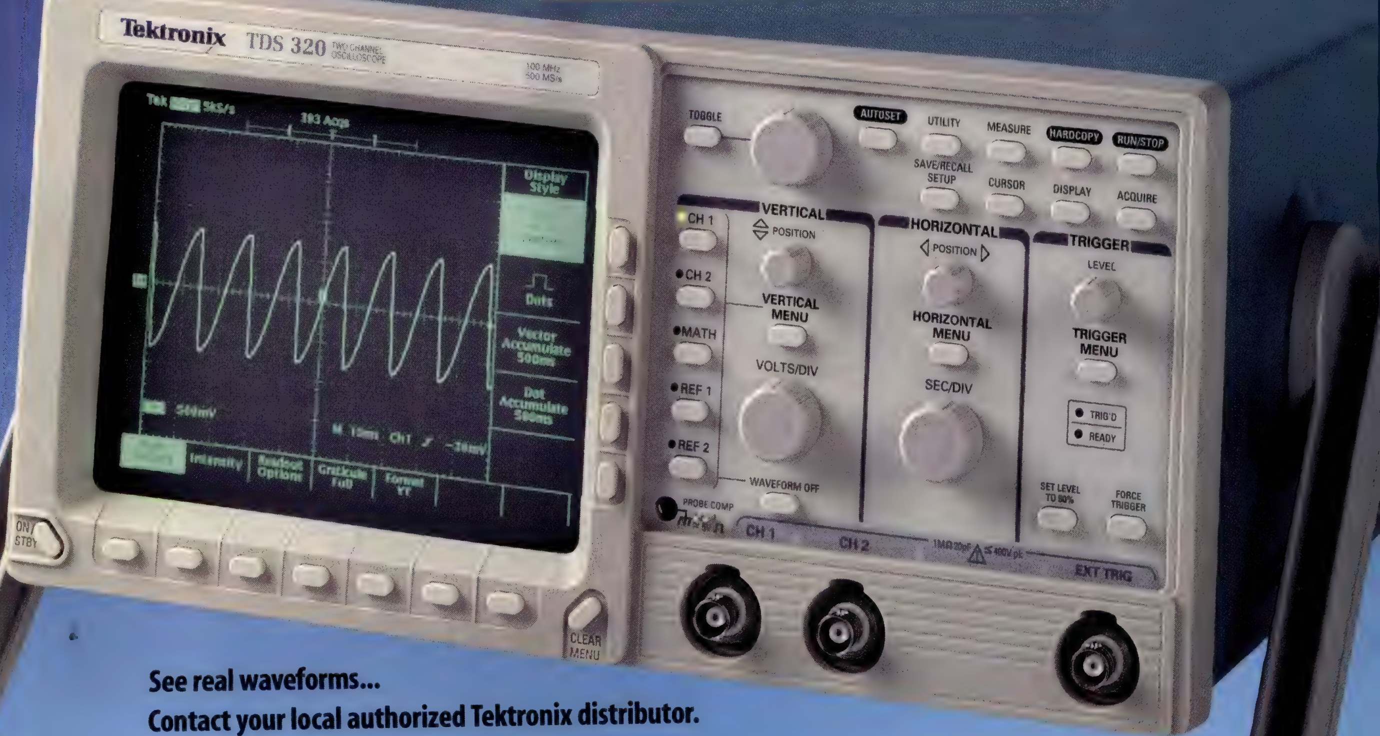
Bandwidth	50 MHz	100 MHz	200 MHz
Max Sample Rate	200 MS/s/chan	500 MS/s/chan	1 GS/s/chan
Sweep Speeds	10 ns/div-5 s/div	5 ns/div-5 s/div	2.5 ns/div-5 s/div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AUTOSET
UTILITY
MEASURE
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RUN/STOP
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CURSOR
DISPLAY
ACQUIRE
VERTICAL
POSITION
CH 1
CH 2
MATH
REF 1
REF 2
VERTICAL MENU
VOLTS/DIV
WAVEFORM OFF
HORIZONTAL
POSITION
HORIZONTAL MENU
SEC/DIV
TRIGGER
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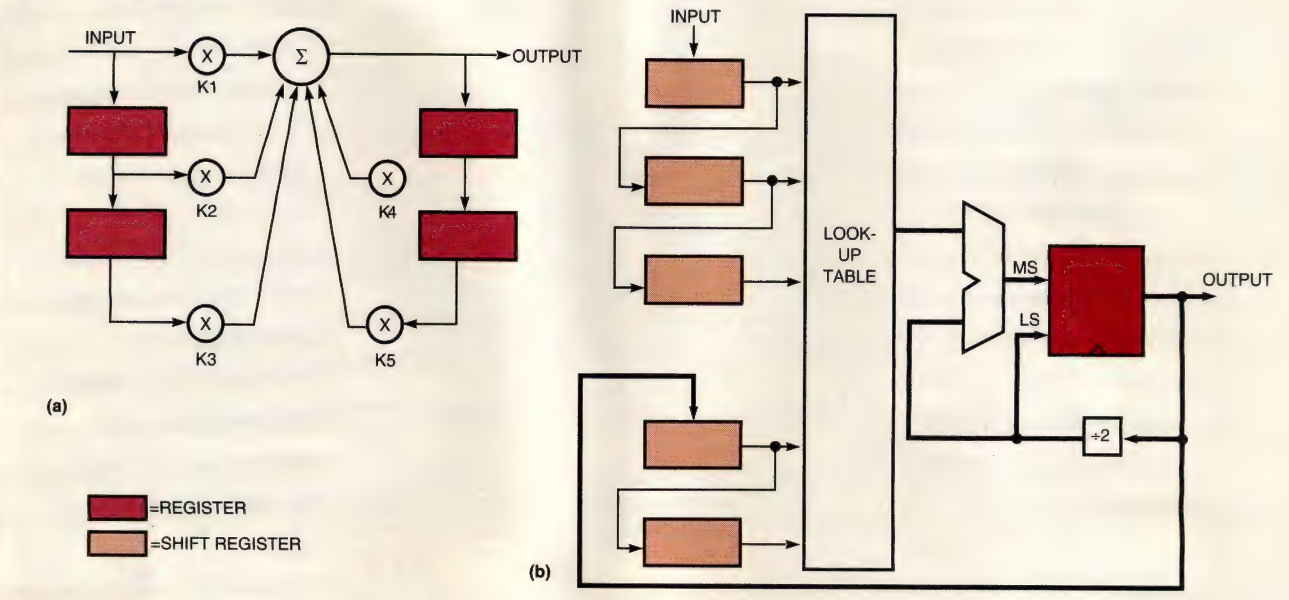
CIRCLE NO. 104

FIGURE 11



A biquad section derives each output from three inputs and two outputs (a). You can obtain a distributed-arithmetic version of a biquad using a 32-word LUT (b)

by entering alternate input samples into separate shift registers. You then interleave the shift-register outputs into the LUTs. Two input-sample times are available for the filter to produce an output. The sample that arrives during the filter cycle is stored and entered at the same time as the one that arrives at the end of the cycle.

IIR filters: IIR filters involve feedback. Each output sample depends not only on current and prior inputs, but also on prior outputs. Consequently, an IIR filter does not reduce arithmetic because you must compute all outputs for internal filter use, even if the filter's output does not required them. You can only approximate linear-phase response because you cannot achieve the ideally symmetrical impulse response that FIR coefficients guarantee. IIR filters are very efficient in terms of filter quality for a given arithmetic bandwidth, however.

A common IIR implementation technique is to cascade small filters instead of building one large filter. Small filters are more stable and are less prone to arithmetic noise. The most common such building block, is the five-coefficient biquad-section filter (**Fig 11**). Biquad sections derive each output from three input samples and two previous outputs. You can conveniently implement a biquad section using a single 32-word LUT. Two shift registers, one from the input and the other from the output, provide LUT addresses. EDN

Acknowledgment

I would like to thank Les Mintzer of Momentum Data Systems and Bruce Newgard of Xilinx for their work on distributed arithmetic that led to this article.

Author's biography

Bernie New has served at Xilinx (San Jose, CA) for four years as a staff applications engineer. His duties include writing application notes, assisting customers, and participating in new-product design. Before joining Xilinx, he served as product-planning manager at Advanced Micro Devices.

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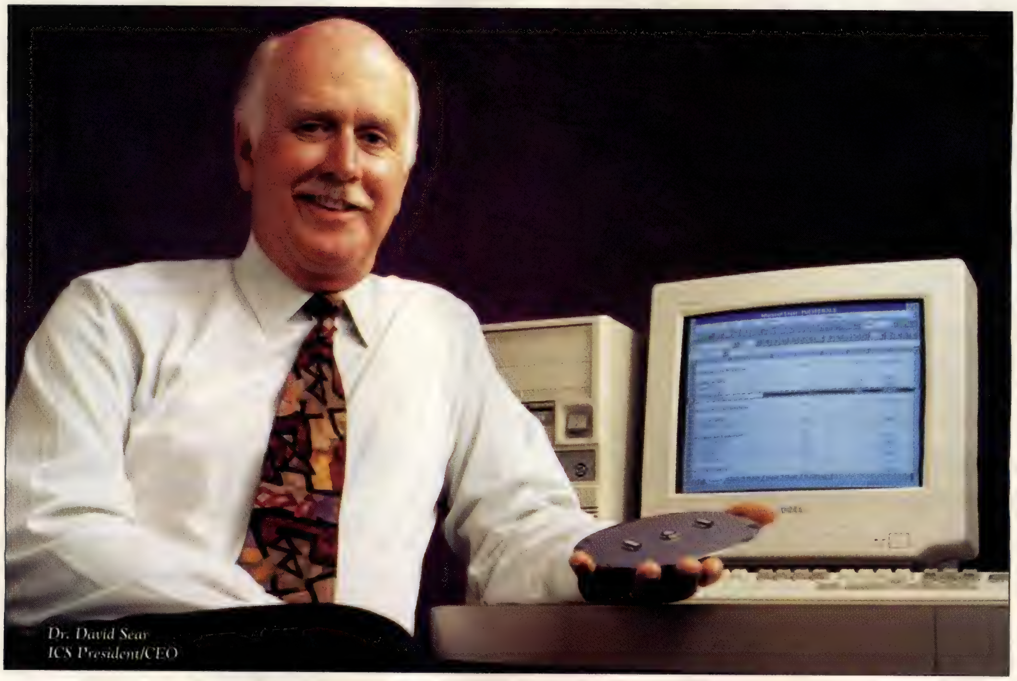
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S/N XXX

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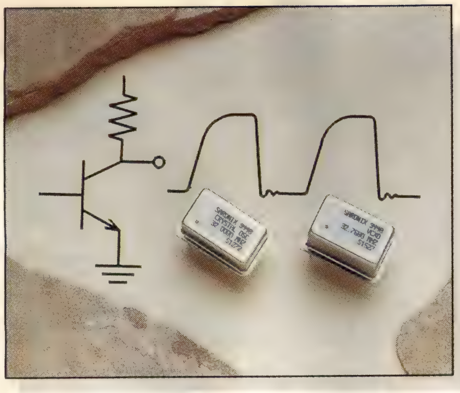
The Model 2930201 oscillator costs $190 (500) and is designed for commercial communications and instrumentation applications. Frequencies range from 5 to 12 MHz. Typical phase noise at 10 MHz is –110 dBc/Hz at 10 Hz, –140 dBc/Hz at 100 Hz, and –160 dBc/Hz at 1 kHz. The aging rate is 5×10^{-10}/day. Frequency stability is $\pm1\times10^{-8}$ over a temperature range of –20 to +60°C. The oscillator measures 2×2×0.75 in. **Piezo Crystal Co,** Carlisle, PA. (717) 249-2151. **Circle No. 392**



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The bipolar TTL S1227 crystal-clock-oscillator line ($1.50 to $4 (1000)) is available in frequencies from 0.5 to 34 MHz. The device is compatible with AT&T's 127-type oscillator family. The oscillators are housed in a 0.2 in.-high, 14-pin, DIP-compatible metal case. The S1527 voltage-controlled, crystal-oscillator line ($13 to $25 (1000)) is available in frequencies from 2.5 to 33 MHz with ±100-ppm minimum frequency shift. The VCXO is housed in a 0.3 in.-high, 14-pin, DIP-compatible metal case. **Saronix,** Palo Alto, CA. (415) 856-6900.

Circle No. 393

VH7126A
-LZ-30
622.08 MHz
RALTRON
9512

622-MHZ VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR FOR SONET AND SDH DATA CONCENTRATORS.

The VH-7126 VCXO is designed for use in 622-MHz PLLs for SONET and synchronous-digital-hierarchy (SDH) data concentrators, telecommunications, and other high-frequency, wide-bandwidth, PLL applications. The devices are available in negative-going ECL outputs and in positive-going positive-ECL outputs. The oscillator has a basic frequency stability of ±15 ppm maximum from 0 to 70°C. Output stability vs load variation is ±0.5 ppm for a load variation of ±10%. An input-control voltage range of 0.5 to 4.5V yields a standard frequency control range of ±70 ppm. Output frequency accuracy at mid-point is ±10 ppm at 25°C. Output jitter is 50 psec p-p. The device costs $80 (1000). **Raltron Electronics Corp,** Miami, FL. (305) 593-6033. **Circle No. 394**

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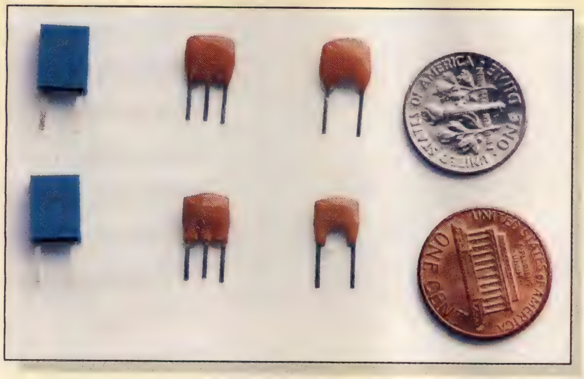

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The ZTS ceramic resonator with built-in capacitor provides a ±0.3% frequency tolerance. The resonators have a frequency range of 2 to 12 MHz and operate down to 1.85V. The operating temperature range is –20 to +80°C. The resonators cost $0.18 (10,000). **Integrity Technology Corp,** Santa Clara, CA. (408) 262-8640. **Circle No. 395**

DIGITALLY COMPENSATED CRYSTAL OSCILLATORS ARE HCMOS COMPATIBLE.

The HDC522 digitally compensated crystal-oscillator family covers the frequency range from 100 kHz to 50 MHz. The units operate from 5V dc and typically draw 40 mA. The output is an HCMOS-compatible square wave with rise and fall times of 6 nsec maximum. Symmetry is 50/50 ±2%. Stabilization is ±0.2 ppm, five seconds after power on. The devices are housed in 24-pin hermetically sealed DIPs. They cost $123.50 (100). **Connor-Winfield Corp,** Aurora, IL. (708) 851-4722. **Circle No. 396**

CLOCK OSCILLATOR MEASURES JUST 1.7×0.9 MM.

The Micro Oscillator 1000 series, a single CMOS IC, needs no quartz crystal or other component for frequency determination. The die measures 1.7×0.9 mm and is available as a bare chip for *chip-on-*board applications or in a standard SO-8 package for surface-mount use. It operates with a frequency stability of 0.5% over 0 to 70°C. Samples are available in SO-8 packages with an operating voltage of 5 V_{CC}. $2.45 (1000). **Micro Oscillator Inc,** Sunnyvale, CA. (408) 984-8139. **Circle No. 397**

300- TO 650-MHZ CLOCK OSCILLATORS HAVE <5-PSEC OUTPUT JITTER.

The M100 clock-oscillator family is available in a 300- to 650-MHz frequency range and provides complementary ECL/positive-ECL clock outputs. The M200/210 family of frequency multipliers has an output frequency range of 300 to 650 MHz. The multiplication factor can range from 2 to 255. Frequency multipliers are useful in systems requiring high-frequency, phase-aligned, synchronous clocks derived from a lower frequency master-clock source. Output-to-reference skew is 1.5 nsec. The M300 family of VCXOs offers an output frequency centered at 622.0800 MHz for use in SONET systems. The devices are housed in 24-pin DIP packages. Typical prices range from $143 to $178 (100). **Micro Networks Corp,** Worcester, MA. (508) 852-5400. **Circle No. 398**

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Low frequency tuning fork Crystal
32.768KHz
20 to 165.0 KHz

CA-301
AT-Strip High frequency Crystal
type 4.0 to 64.0 MHz

CIRCLE NO. 106

SMD

MC-405/6
Heat resistive C-2H Crystal
L10.4xW4.06xH3.56mm
20 to 165 KHz

MA-406 & MA-505/6
Heat resistive CA-303 Crystal
4.0 to 64.0 MHz

32.768K
6971A

CIRCLE NO. 107

MINI-SMD

MC-306
Miniature AT-strip Technology
EPSON tuning fork Crystal
L7.0xW3.8xH2.5mm
32.768 KHz

MA-306
Miniature AT-strip Technology
L7.9xW3.8xH2.5mm
17.7 to 40.0 MHz

CIRCLE NO. 108

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RTC
72421A 9132

RTC-4553
Serial data bus,
miniature package,
user RAM (30x4bit).

RTC-58321/3
4 bit parallel bus,
I/O connection.

RTC-62421/3
4 bit parallel bus,
low standby current
consumption.

RTC-72421/3
4 bit parallel bus,
low standby current
consumption.

RTC-63421/3
4 bit parallel bus,
alarm function.

RTC-64611
8 bit parallel bus,
alarm function.

RTC-65271
8 bit parallel bus,
4K bytes SRAM,
battery holder.

RTC-658x
8 bit parallel bus,
114 bytes SRAM,
battery holder.

RTC-659x
8 bit parallel bus,
114 bytes SRAM,
battery holder, alarm.

CIRCLE NO. 109

Oscillators

Latest technology Epson Crystal Oscillators

THROUGH HOLE

SG-51
Full size
Auto insertable
1.025 to 125.0 MHz

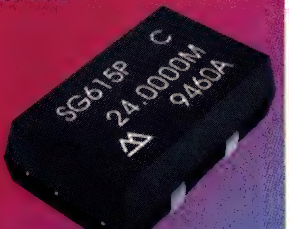
SG-531
Half size
Auto-insertable
1.025 to 125.0 MHz

SG51 813
16.0000MHz C

CIRCLE NO. 110

SMD

SG-615
Internal heat resistive CA-303 Crystal
L14.0xW9.8xH4.7mm
1.025 to 125.0 MHz



CIRCLE NO. 111

MINI-SMD

SG-636
Miniature AT-strip Technology
L10.3xW5.8xH2.8mm
2.20 to 80.0 MHz

18.432D C
PTF2180A

CIRCLE NO. 112

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Voltage regulator offers 1% accuracy and 1.2V drop. The LD117 voltage regulator provides up to 800-mA output current and is available in a variable 1.2 to 18V output version and fixed outputs of 5.5, 2.85, 3, 3.3, and 5V. The device has internal current limiting and thermal protection. The only external components required are 100-nF and 10-μF capacitors. Maximum input voltage is 20V dc. The regulator is available in TO-220, SOT-223, SO-8, and DPAK packages. From $0.75 (1000). **SGS-Thomson Microelectronics**, Lincoln, MA. (617) 259-0300.

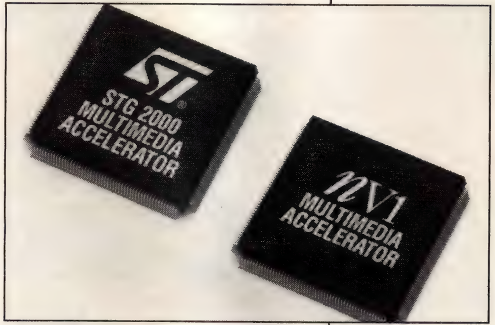
Circle No. 358

Instrumentation amplifier has 5-fA typical bias current. The INA116 is a monolithic FET-input instrumentation amplifier. The three-op-amp design provides a high-impedance differential input and allows gain setting from 1 to 1000 using a single external resistor. The amplifier operates from ±4.5 to ±18V supplies and has a 1-mA quiescent current. Buffered guard connections are provided adjacent to each input for achieving low-leakage pc-board designs. The device has a 2-mV maximum offset voltage, 84-dB common-mode rejection at a gain of 10, and ±40V input overvoltage protection. In 16-pin DIPs or SOL packages, the amplifier costs $6.95 (1000). **Burr-Brown Corp**, Tucson, AZ. (602) 746-1111.

Circle No. 359

Clock generator for Nx586 CPU. The ICS9159-07 clock-generator chip is designed for use with NexGen's NX586. The device supplies all typical PC motherboard clocks from a single 14.318-MHz crystal source. Outputs include three copies of the processor clock, seven copies of the PCI bus clock, the system reference clock, a floppy-drive adapter clock, and a keyboard controller clock. The chip accommodates dynamic switching of the frequencies with smooth transition to the new frequencies. The device does not violate the CPU's timing specifications. Maximum output frequency is 65 MHz in either 5 or 3.3V operating mode. The clock generator is housed in a 28-pin SOIC package and costs $2.90 (10,000). **Integrated Circuit Systems Inc**, San Jose, CA. (408) 297-1201.

Circle No. 360



▲ **Multimedia accelerators for graphics and audio.** The STG2000 and NV1 deliver real-time realistic 3-D graphics, video-based special effects, full-motion video acceleration, and concurrent high-fidelity audio. The chips were developed through a partnership between SGS-Thomson Microelectronics and NVIDIA Corp (Sunnyvale, CA). The STG2000 DRAM multimedia accelerator and its companion palette DAC, the STG1732, cost $55 (OEM). The NV1 VRAM multimedia accelerator and companion palette DAC are available from NVIDIA and cost $70 (OEM). **SGS-Thomson Microelectronics**, Lincoln, MA. (617) 259-0300.

Circle No. 361

Low-power, high-bandwidth amplifiers for battery-powered applications. The EL2270C series includes single-, dual-, and quad-current-mode feedback amplifiers with a –3-dB bandwidth of 70 MHz. Power consumption is approximately 1 mA per amplifier. The outputs can drive up to 55 mA and swing ±4V. The EL2170C single amplifier can output 100 mA. The devices operate from a single 3V supply or dual supplies up to ±6V. The outputs can swing within 1V of either supply. Typical differential phase is 0.15°, and differential gain is 0.15% into a 150Ω load. From $1.99 (1000). **Elantec Inc**, Milpitas, CA. (408) 945-1323.

Circle No. 362

Chip set for low-power pen-input systems. This 3V chip set comprises the W6004F and the W70-03F analog/digital electromagnetic system. The chip set is based on the company's patented electromagnetic-resonance technology, which allows battery-free electronic pen operation. According to the company, the pen system offers high data rates, high resolution, accuracy, proximity sensing, and pressure sensitivity. The chips are housed in 100-pin TQFPs; the set costs $50 (100,000). **Wacom Technology Corp**, Santa Clara, CA. (408) 982-2727.

Circle No. 363

Facsimile modem chip sets integrate multiple functions. The Extended Faxengine (XFE) family of modems integrate all the control functions of a combined facsimile, digital answering machine, and full-duplex speakerphone into a two-device set. The chip sets let you develop thermal and plain-paper fax machines. The facsimile modems include synchronous, half-duplex modems designed for Group 3 facsimile operation over standard telephone lines. They operate at 9600 bps and 14,400 bps, satisfying ITU standards V.29 and V.17. The R96XFE-MVPS, a member of the XFE family, costs $45 (10,000). **Rockwell Telecommunications**, Newport Beach, CA. (800) 436-9988.

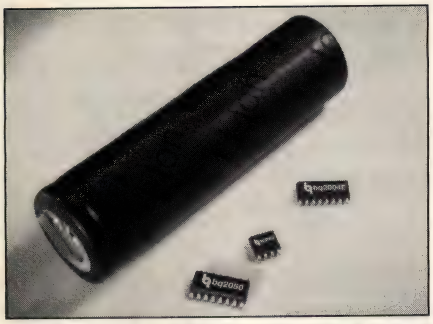
Circle No. 364

Parallel synchronous FIFOs operate at 50 MHz. The QS72215 has 512×18 configuration, and the QS72225 has a 1024×18 configuration. Both devices are pin-compatible with the IDT72215LB/25LB FIFOs. The devices use an internal memory based on CMOS dual-port SRAM technology. The FIFOs have synchronous clocks at both input and output ports. Both devices are available in cycle times of 20, 25, or 35 nsec. Housed in a 68-pin PLCC, the 35-nsec QS72215 costs $18.75 (1000), and the 35-nsec QS72225 costs $24.17 (1000). **Quality Semiconductor Inc**, Santa Clara, CA. (408) 450-8080.

Circle No. 365

Low differential phase/gain-error video multiplexers. This video-multiplexer family comprises the 1×1 MAX4111, the 2×1 MAX4121, the dual 2×1 MAX4221, and the 4×1 MAX4141. Key specifications include a differential phase error of 0.01°, a differential gain error of 0.01%, a 0.1-dB bandwidth of 80 MHz, and –3-dB bandwidth of 330 MHz. Off isolation is –74 dB, and crosstalk is –66 dB at 30 MHz. The multi-

plexers have a constant high input impedance, which is independent of the switch connection, and high output impedance when in the disabled state. The unity-gain devices have a full power-bandwidth slew rate of 700 V/µsec. They drive capacitive loads without oscillation. From $1.70 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087.
Circle No. 366



ICs for charging, monitoring, and cell-supervising Li-ion batteries. The bq2050 provides accurate state-of-charge information in either milliampere or milliwatt hours over a range of environmental conditions. The 16-pin device can measure current, battery temperature, and battery voltage. The bq2050 costs $4.84 (10,000). The bq2053 is a battery-pack supervisor configurable for two, three, or four series cells. It draws <15 µA and protects the Li-ion pack from overvoltage and undervoltage; the bq2053 limits charging and discharging to prevent accidental short circuits or overcurrent situations. Housed in an eight-pin DIP or SOIC, the device costs $1.46 (10,000). The bq2004E charges both NiCd and nickel-metal-hydride batteries and can be configured for Li-ion charging. Housed in a 16-pin DIP or SOIC, the device costs $3.59 (10,000). **Benchmarq Microelectronics Inc**, Dallas, TX. (214) 437-9195.
Circle No. 367

0.65-µm, 5V gate-array family. The CMOS ASIC product family includes the CG46 digital CMOS gate array and the CE46 embedded array, which supports diffused high-speed RAMs and ROMs. The product family features a pin-to-gate ratio of 115 to 182 and up to 89,000 usable gates in a channel-less sea-of-gates architecture. I/O-pad count ranges from 208 to 400. The company's proprietary-clock-distribution system minimizes clock skew to as low as 400 psec. The series supports system clock speeds up to 70 MHz and has a 175-MHz toggle frequency. Average power consumption is 4.5 µW/gate/MHz. NRE cost starts at $40,000. A CG46F40, which provides 45,000 usable gates in a 208-pin PQFP, costs $12.50 (100,000). **Fujitsu Microelectronics Inc**, San Jose, CA. (408) 922-9000.
Circle No. 368

Copper Gbaud link module. The VSC7181 GLM copper-based module complies with the HP-IBM-Sun Fibre Channel System Initiative (FCSI), 1.0625-Gbps, Gigabaud Link Module (GLM) specification. The module interfaces with the system through a 20-bit 8B/10B encoded 53-MHz TTL bus, as defined by the Fibre Channel GLM specification. Compliance with the standard means a single system can use

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CIRCLE NO. 84

copper for distances <50m or use fiber optics for longer distances. The module costs $200 (1000). An evaluation kit costs $995. **Vitesse Semiconductor Corp,** Camarillo, CA. (805) 388-3700. **Circle No. 369**

Low-dropout voltage regulator has low quiescent current. The LK115D linear regulator has a dropout voltage of 0.2V and is available in fixed output voltages of 2, 2.5, 3, 3.3, 4, 4.75, 4.85, 5, and 5.5V. Typical quiescent current in off mode is 0.01 μA (1 μA max) and in on mode is 280 μA. The regulators have both active-high and active-low shutdown-control pins for design flexibility. All devices are specified for operation from –40 to +125°C and have a maximum input voltage of 20V dc. Housed in an SO-8 package, the devices require only a single 2.2-μF capacitor for stability. $0.39 (1000). **SGS-Thomson Microelectronics,** Lincoln, MA. (617) 259-0300. **Circle No. 370**

Low-dropout linear regulator has 500-mA output current. The LT1175 draws 45 μA of quiescent current, dropping to 10 μA in shutdown mode. Dropout voltage is 0.5V at full load current, dropping to 0.1V at 100 mA. You can select a current limit of 200, 400, 600, or 800 mA using two external pins. The device is available in an SO-8 or five-lead DD surface-mount package or a TO-22 through-hole package. Fixed-5V and adjustable-output-voltage versions are available from $2.90 (1000) (SO-8 package). **Linear Technology Corp,** Milpitas, CA. (408) 432-1900. **Circle No. 371**

Monolithic stereo audio amplifier has 20W output per channel. The LM1876TF has performance rivaling discrete amplifiers with 0.1% typical THD plus noise from 20 Hz to 20 kHz. On-chip muting has a fade-in and -out feature that avoids audio pops or clicks. Internal protection makes the IC nearly impervious to damage from instantaneous temperature peaks, overvoltage, undervoltage, and overloads. Current consumption in standby mode is 6 mA max. The device is housed in a 15-lead TO-220 isolated package and costs $3.20 (1000). **National Semiconductor Corp,** Santa Clara, CA. (800) 272-9959. **Circle No. 372**

Bus-master PCI-to-IDE controller chip. The PCI0646 PCI-to-IDE controller chip works with any enhanced-IDE and fast-ATA-2 hard drive or ATAPI CD-ROM with full plug-and-play compliance. According to the manufacturer, the device provides a 30% performance improvement over previous controllers. The chip costs $6 (OEM). **CMD Technology Inc,** Irvine, CA. (714) 454-0800. **Circle No. 373**

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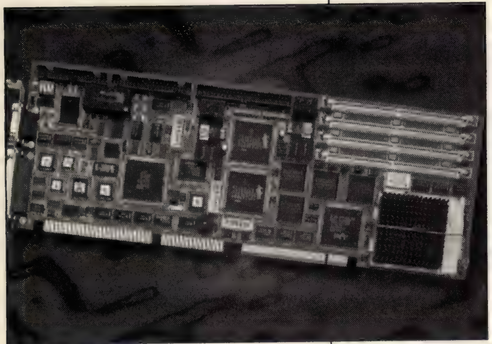
Circle No. 375



▲ Pentium-based single-board computer for PCI/ISA or ISA passive backplane systems. The P590 is based on the 90-MHz Pentium processor and provides interfaces to PCI, ISA, SCSI, and IDE. The board complies with the PCI spec-ification for passive-backplane PCs developed by the PCI Industrial Computer Manufacturers Group (PICMG). It acommodates up to 512 kbytes of synchronous-burst-SRAM secondary cache and up to 128 Mbytes of DRAM. The board has two 16550-compatible RS-232C ports and a parallel port. The board costs $2695. **Texas Microsystems Inc**, Houston, TX. (713) 541-8200.
Circle No. 376

ICE for Motorola 68307 μP. The HMI-200-68307 in-circuit emulator (ICE) provides real-time emulation for the 3.3 or 5V versions of the 68307 operating at speeds as high as 16 MHz. A high-speed RS-232C interface provides communication between the host computer and emulator with a parallel port for faster code downloading. An optional Transmission Control Protocol/Internet Protocol-based Ethernet interface is also available. The unit comes standard with 256 kbytes of overlay memory with options for 1, 2, or 4 Mbytes. The system includes a high-level language debugger for C and Ada. A hardware-performance-analysis system is optional. The basic system is $12,000 for PCs and $13,000 for Sun and HP workstations. The performance-analysis option is $2500; the Ethernet interface costs $1500. **Huntsville Microsystems Inc**, Huntsville, AL. (205) 881-6005.
Circle No. 377

Interactive-analysis and visualization package for Windows. O-Matrix 2.1 for Windows, according to its maker, combines the programming flexibility and performance of a compiled language with the ease of use and functionality of an integrated environment. In addition to analysis and graphics capabilities, the tool has an integrated debugger, a profiler, a full-screen editor, and a matrix-oriented interpreted language. The interactive environment takes advantage of the 32-bit PC architecture for increased performance. The software costs $395. **Harmonic Software Inc**, Seattle, WA. (800) 895-4546.
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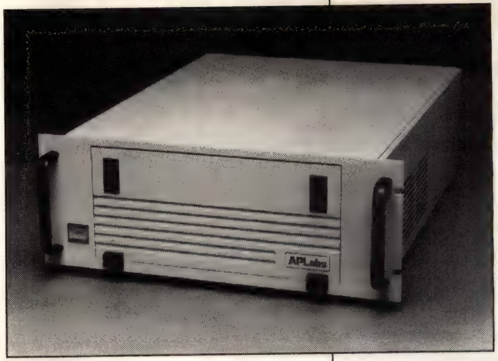

▲ Ruggedized, rack-mount enclosure. The ruggedized rack-mount 4U workstation/SCSI enclosure works alone or as a companion component to the company's VMEstation workstation. It offers optional EMI/RFI conformance to MIL-STD-461 for laboratory environments. In its normal configuration, the enclosure houses a workstation, such as a Sun SPARCstation 20, Sun SPARCstation 5, Silicon Graphics Indy Series, or DEC Alpha-based CPUs, plus up to six 3.5-in. peripherals. You can also use the enclosure without a workstation to house as many as 12 3.5-in. peripherals. The enclosure is wired with a 375W power supply and uses dc-fan convection cooling. It costs $2995. **AP Labs Inc**, San Diego, CA. (619) 546-8626. **Circle No. 379**

486-based CPU card has full 16-bit ISA compatibility. The 7000 CPU card operates in a passive backplane and can be used standalone or with Micro PC expansion cards. The 4.5× 4.9-in. CPU card has a 25-MHz 486SLC processor with built-in primary cache. Three solid-state disks function as DOS drives for the user, providing a total storage capacity of 2.5 Mbytes. Other features include 4 to 8 Mbytes of DRAM, an 80387SX coprocessor socket, two 16C550-compatible serial ports with an RS-232C/RS-485 interface, an LPT1 bidirectional parallel port, a watchdog timer with a time-out of 1.2 sec, an AT-style clock calendar, and keyboard and speaker ports. $700 (OEM qty). **Octagon Systems**, Westminster, CO. (303) 430-1500.
Circle No. 380

Flat-panel computer subsystems. The TEK-PAK line of flat-panel computer subsystems comes with a 386SX to 486DX4 single-board computer and a NEMA-4-rated front panel with either a passive-matrix STN or an active-matrix TFT, 10.4-in. color display. The system enclosure has a ruggedized, open frame design that is easy to mount and facilitates adding peripheral expansion cards at the OEM or end-user level. The TEK-PAK can also be configured with a 2.5-in. hard drive and an optional capacitive or resistive touch screen. The company provides all interface hardware and software. A 486SX-25 passive matrix color system with 290-Mbyte hard disk costs $4395. **Teknor Microsystems Inc**, Boisbriand, PQ, Canada. (514) 437-5682.
Circle No. 381

VME processor board uses PowerPC 603. The Power3 VMEbus board has a PMC/PCI local mezzanine bus and VME64 interface. It provides a 512-kbyte secondary cache for the Motorola PowerPC 603 processor and up to 256 Mbytes of DRAM. I/O

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includes Ethernet, SCSI-2, keyboard port, mouse port, two RS-232C ports, Centronics parallel port, and floppy-disk I/O ports. The board provides two sockets for either flash memory or EPROM. It meets the IEEE-1275 standard for Boot Firmware, the PCI Local Bus and IEEE-P1386 Proposed Standard for a Common Mezzanine Card Family, and the PowerPC Common Hardware Reference Platform standard. The basic configuration costs $4000. **VI Computer Corp**, Encinitas, CA. (619) 632-5823. **Circle No. 382**

Real-time emulators support Microchip's PIC-16Cxx microcontrollers. The PB-64 probe card supports the PIC16C64 microcontroller, and the PB-74 probe card supports the PIC16C74 microcontroller. The probe cards work with the RICE16 PIC real-time emulator, which also supports the PIC16C5x family and other PIC16Cxx microcontrollers. The probe cards use emulator bond-out chips from Microchip and provide real-time emulation to 12 MHz. An emulator cable plugs into a 40-pin, dual-in-line socket in the target system. The RICE16 emulator connects to a PC via the parallel printer port and runs under MS-DOS. The probe cards cost $475 each. **Advanced Transdata Corp**, Dallas, TX. (214) 980-2960. **Circle No. 383**

Development system for VLSI fuzzy-logic processor. FuzzyStudio consists of an application-development board that connects to a standard PC via an RS-232C port and a Windows-based software-development tool. The hardware and software let you program the Weight Associative Rule Processor (WARP1) using intuitive graphical and linguistic methods. The system costs $2000. **SGS-Thomson Microelectronics**, Lincoln, MA. (617) 259-0300. **Circle No. 384**

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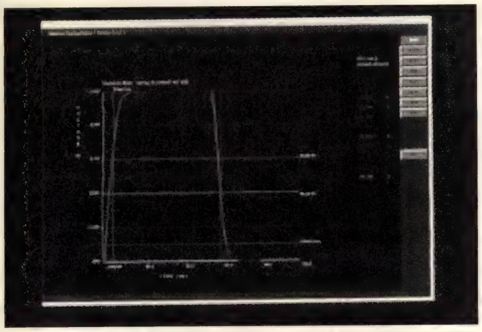
System simulator adds analysis and block-processing tools for DSP and communications. SystemView version 1.8 has an analysis window for detailed analytic examination of spectra and waveforms. You can select outputs from locations within the system design for display in 2-D plot windows. A sink calculator performs block processing on sink data that system simulation generates. Typical processing operations include auto- and cross-correlation, windowed spectral analysis, algebraic operations, eye patterns, histograms, statistical overlays, and waterfall displays. The tool also lets you cascade block operations. SystemView 1.8 costs $2450. Optional libraries for communications, DSP, logic, and RF start at $525. **Elanix Inc**, Westlake Village, CA. (818) 597-1414. **Circle No. 344**



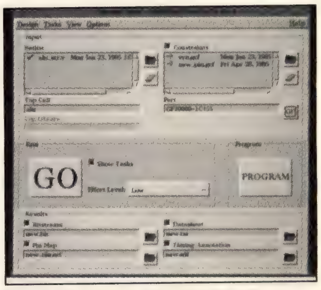
▲ **Signal-integrity tool for submicron ICs.** VLSI Signal Integrity helps designers of full-custom and semicustom ICs, including ASICs, analyze designs for crosstalk, wave-propagation delay, and clock skew. It also helps analyze designs for high-frequency signal noise, provides power-distribution information for the power bus or plane, and simulates accurate interconnect delays with back-annotation to the logic simulator. The tool uses 2- and 3-D electromagnetic field solvers for parasitic-parameter extraction and a Spice analog simulator for lossy coupled transmission lines. US license fees start at $20,000. **Pacific Numerix Corp**, Scottsdale, AZ. (602) 483-6800. **Circle No. 345**

DSP development kit for ICs designed for wireless applications. The COSSAP TMS320C54x DSP development kit allows you to design TMS320C541 or TMS320C542 DSPs and cores into electronic systems and ASICs for wireless-communication applications. The development kit includes a full instruction-level simulator with interactive debugging capabilities. Software-development tools (from TI) for the company's DSPs and cores are also included in the kit. The development kit costs $7500. To accelerate system-level design, the COSSAP DSP design environment integrates hardware-software codesign, cosimulation, and system-level verification. The COSSAP DSP-design-automation environment starts at $30,000. **Synopsys**, Mountain View, CA. (415) 962-5000. **Circle No. 346**

Data-path-synthesis tool optimizes at the function level. The PathBlazer data-path-synthesis tool explores all architectural options for a complex data path and considers placement. Function-level optimization lets the tool explore architectural trade-offs that would ordinarily be lost at the gate level. Function-level optimization can also operate faster than synthesis tools that operate at the Boolean level. The tool will be available for Unix-based systems and will be shipped in the fourth quarter. It costs $40,000. Viewlogic markets, sells, and supports the tool, which is a product of Silerity. **Viewlogic Systems Inc**, Marlborough, MA. (508) 480-0881. **Circle No. 347**

Analog simulation environment for complex-system and IC design. AnalogView provides you with design entry; the ability to manage multiple, complex simulation runs; and the ability to collect and postprocess results. The tool lets you assign input stimuli, command controls, analysis types, and probes for current and voltage. The tool also lets you invoke the simulation and analyzer results from a common environment. The environment is initially available for HSpice and ViewSpice. It costs $7500. **Viewlogic Systems Inc**, Marlborough, MA. (508) 480-0881. **Circle No. 348**

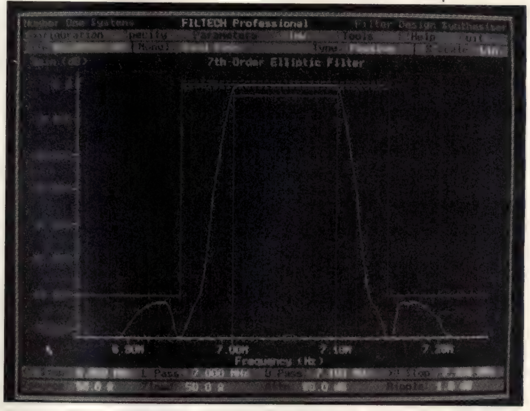
FPGA-design tool provides deterministic timing. The Designer Series 3.0 tool set features a graphical user interface and object-oriented database to simplify the design of complex field-programmable gate arrays (FPGAs). The tool set's DirectTime option ensures that preroute-specified timing delays appear accurately in the final design. The DesignScript tool provides a macro language that lets you run the design process as a batch command, saving a series of design steps, such as compile, place, route, fuse, extract, and back-annotate, in a script file. Designer Series 3 costs $995 and accommodates 2500-gate designs. Designer Advantage 3.0 accommodates all the vendor's FPGAs and costs $2495 in a PC version and $3495 in a workstation version. The DirectTime option costs $995. **Actel Corp**, Sunnyvale, CA. (408) 739-1010. **Circle No. 349**



FPGA family offers as many as 51,000 gates. The GF100K field-programmable gate-array (FPGA) family is initially available with 9000- and 51,000-gate devices. The company expects to offer 23,000-, 35,000-, and 100,000-gate devices by year-end. The flash-based devices use the company's Desktop Foundry electronic-design-automation tools to perform partitioning, placement, and routing. The tools also provide design kits that support Verilog, VHDL, Electronic Design Interoperability Format, and standard-delay-format industry standards. Design kits also support schematic capture; logic synthesis; and simulation programs from Cadence, Mentor, Synopsys, and Viewlogic. The GF9K device costs $30 (25,000), and the GF51K costs $900 (3000). Desktop Foundry and a hardware-description-language-design kit cost $16,500. Desktop Foundry with a Mentor Graphics schematic-design kit costs $10,000. **GateField, a Zycad Corp**, Fremont, CA. (510) 249-5757. **Circle No. 350**

Cycle-based simulator supports full VHDL. The Ultraspec cycle-based simulator achieves simulation speeds as much as 100× faster than traditional VHDL simulators. The product combines a cycle-based simulator with the company's full VHDL technology. Because it supports the full VHDL language, the simulator prevents the need for you to code style to take advantage of the cycle-based simulation speed. The simulator costs $55,000, and the company expects to begin production shipments in the fourth quarter. **Vantage Analysis Systems Inc**, Fremont, CA. (510) 659-0901. **Circle No. 351**

Program designs and documents hardware for 8-bit CPU systems. MicroBench lets you convert product ideas into operating hardware. The tool runs under Windows and guides you through the selection of operational functions to create microcontroller-based products. The program generates a programmed, 8-bit CPU and hardcopy documentation, including system block diagrams, circuit schematics, parts lists, program listings, and assembly-level object codes. The tool has preprogrammed functions and associated circuits for those functions stored in libraries. The library functions include analog and digital inputs and outputs, visual readouts, and memory. The initial release uses Microchip Technology's PIC devices. It costs $695. **MicroBench Software Inc**, Sunnyvale, CA. (408) 248-7776. **Circle No. 352**



▲ **Filter-circuit synthesis program.** Filtech Professional helps you design passive and active filters to the twelfth order. The program includes a built-in circuit simulator that lets you immediately test the circuit and compare the filter's response with your specifications. You can specify filters by designating the frequency limits, the stopband attenuation required, and the maximum acceptable passband ripple. You can also vary component values and select among Bessel, Butterworth, Chebyshev, or Elliptic filter types. $475. **Number One Systems**, Los Altos, CA. (415) 968-9306. **Circle No. 353**

ATPG tool offers critical-path test capabilities. The FastScan automatic-test-pattern-generation (ATPG) tool now provides ATPG for critical paths embedded in scan-based ASIC, IC, and multichip-module designs. The test patterns can verify device performance and detect ac-manufacturing defects. FastScan costs $92,400, and prices for the critical-path test option start at $25,000. **Mentor Graphics**, Wilsonville, OR. (503) 685-8000. **Circle No. 354**

High-level design-automation tool extends ASIC design capabilities. The enhanced DesignBook features improved support for ASIC designers using VHDL or Verilog hardware-description languages (HDLs) and Synopsys' synthesis tools. The software simplifies design functions, such as capturing the design intent, generating synthesizable HDL code from documentation-type source code, developing a test bench, and trying coding styles and synthesis-tool settings to meet design goals. The software, initially available on PCs, is now available for Unix systems. Prices for Unix versions start at $17,000. **Escalade**, Sunnyvale, CA. (408) 481-1300. **Circle No. 355**

Verilog and VHDL simulators combine in a co-simulation tool. Verilog/QuickVHDL merges Cadence's Verilog-XL and Mentor Graphics' QuickVHDL into one tool. The combination lets you use a single hardware-description language for design descriptions and lets you use models from both languages. The software runs on Sun and HP 9000 workstations and costs $12,000 for a node-locked license and $16,000 for a single-user floating license. **Precedence Inc**, Santa Clara, CA. (408) 345-4880. **Circle No. 356**

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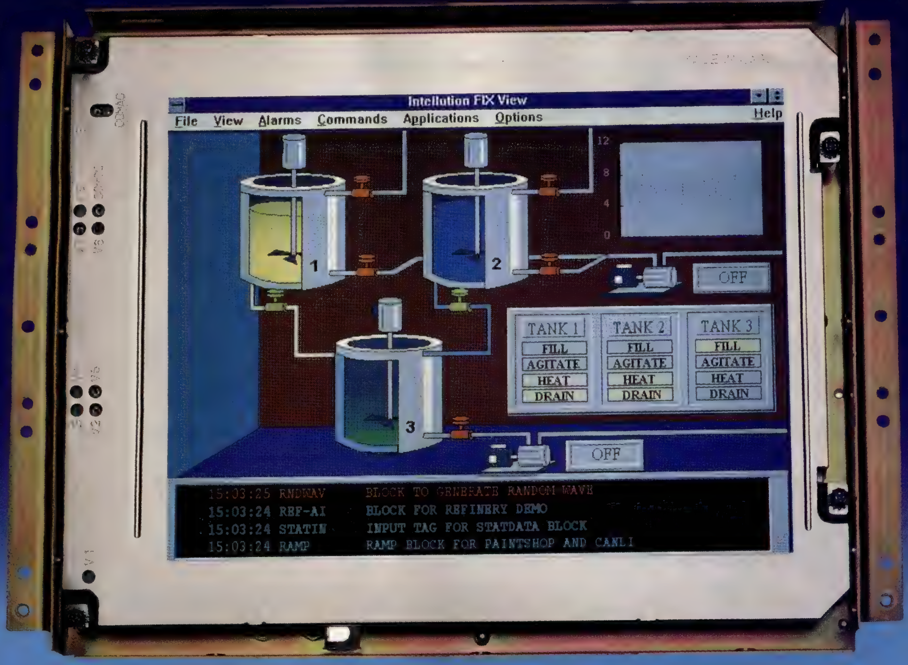

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15:03:25 RNDWAV    BLOCK TO GENERATE RANDOM WAVE
15:03:24 REF-AI    BLOCK FOR REFINERY DEMO
15:03:24 STATIN    INPUT TAG FOR STATDATA BLOCK
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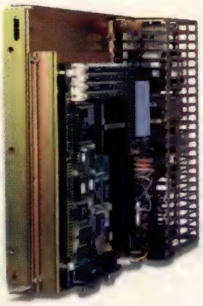

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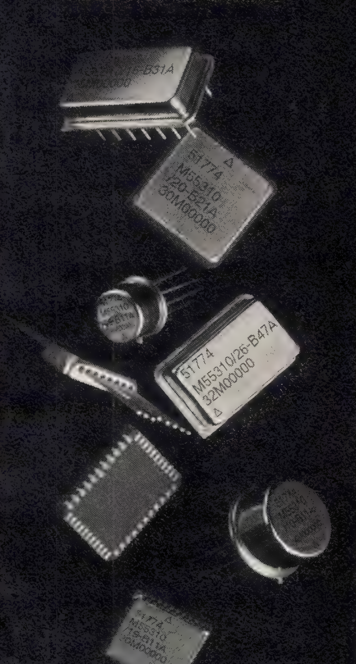

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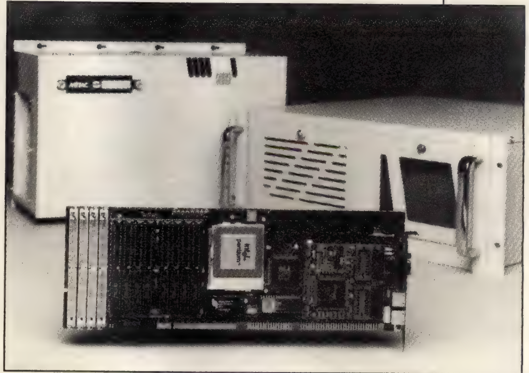
PCI-based high-performance computing subsystems. The AL860-PCI and the FT200-PCI suit image processing, DSP, and other computation-intensive operations. You can configure a single board for 50 to 200 MFLOPS or several boards for several GFLOPS of computing power. Each board is configurable with up to 256 Mbytes of memory and high-performance I/O cards. Both boards support burst transfers at 132 Mbytes/sec and sustained transfer of 70 Mbytes/sec. The I/O cards support high-resolution displays, digital-camera interfaces, frame-grabber interfaces, SCSI, and high-speed digital I/O at sustained rates up to 160 Mbytes/sec. Prices for the AL860-PCI Series start at $3995, and prices for the FT200-PCI Series start at $8495. **Alacron**, Nashua, NH. (603) 891-2750. **Circle No. 328**



▲ **Pentium single-board computer for PCI/ISA bus.** The MSC-252 is available with a range of CPUs, including Intel's 75/90/100-MHz Pentium processors and the Cyrix M1 CPU. The board includes Peripheral Component Interconnect (PCI)-based video with 32-bit display memory for standard and extended video modes up to 1280×1024-pixel resolution with 256 colors, two PCI IDE hard-disk-controller ports, a floppy-disk-drive-controller interface, a bidirectional parallel port, and two high-speed RS-232C ports. The board also includes a 10-stage watchdog timer, a real-time clock, onboard post-LED indicators, password protection, and a PS/2 keyboard and mouse connector. Prices for the single-board computer start at $2495. **Mitac Industrial Corp**, Fremont, CA. (510) 656-5288. **Circle No. 329**

Analog capacitive touchscreens with color monitors. The touchscreen monitors come with an analog capacitive touch panel, a mouse driver, controller and cables, VGA and SVGA resolution, and an unlimited color display. The capacitive touchscreens can communicate 270 touch points/sec at 19.2 kbaud and are rated for more than 20 million touches in any location. The 10-in. VM-10T monitor costs $999, the 14-in. VM-14T costs $799, the 15-in. VM-15T costs $1099, and the 17-in. VM-17T costs $1599. **ETC Computer Inc**, Fremont, CA. (510) 226-6250. **Circle No. 330**

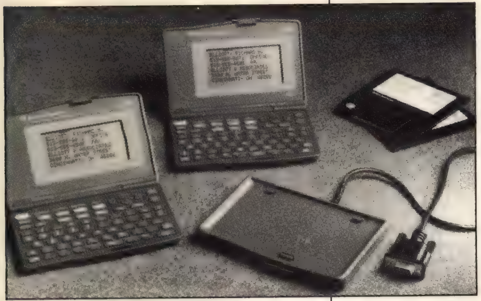
Bootable PC Card reader adds removable C drive to industrial computers. The ATA/B-R PC Card reader lets ruggedized PCMCIA-ATA flash cards and 1.8-in. hard drives function as a removable C drive in industrial-computing applications. The system permits users in harsh or high-security environments to remove their systems, including the operating system, applications, and data by ejecting the PC Card. It costs $79. **ProTege Corp**, Irvine, CA. (714) 450-8950. **Circle No. 331**

Software allows full-duplex voice communication over the Internet. Digiphone provides ordinary two-way voice communication over the Internet using a 386 PC running Windows and a 9600-bps modem. The software allows voice and data encryption, and on-the-fly adjustment of data compression. It costs $149.95. **Camelot Corp**, Dallas, TX. (214) 713-2607. **Circle No. 332**

CD-ROM drive has 6X speed, offering 110-msec seek time. The 6X CD-ROM drive has an in-circuit-emulator/AT-attachment-packet interface and transfers data at 900 kbytes/sec. The drive plays 2X, 3X, and 4X CD-ROM titles and is ready for CD-ROM XA. It is compatible with Kodak Multi-Session photo CDs and MPC Level 2.

The 5.25-in. drive has a 256-kbyte buffer and costs $549. **Teac America, Data Storage Products Division**, Montebello, CA. (213) 726-0303.
Circle No. 334

Device converts CD-ROM drives from single to wide SCSI differential. The RTSDA-PW mounts directly onto a Plextor 4Plex or 6Plex CD-ROM drive. The device-independent peripheral converter requires no software to operate. According to the company, the device is adaptable to most CD-ROM drives. The converter costs $180 (100). **Rancho Technology**, Rancho Cucamonga, CA. (909) 987-3966. **Circle No. 335**



▲ Personal organizers provide docking-station connectivity to PCs. The PS-6800 with 128 kbytes of memory and the PS-6700 with 64 kbytes of memory use the PS-6155 docking station and Windows software to connect with a PC. The PS-6700 costs $69, the PS-6800 costs $89, and the PS-6155 costs $49.95. **Texas Instruments Inc**, Temple, TX. (800) 842-2737.
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Reference design combines video, capture, MPEG playback, and TV tuning on a single board. The RedFox reference design uses the company's VxP501 capture and playback processor and C-Cube's CL480PC Moving Pictures Experts Group (MPEG) 1 System decoder. According to the company, the total bill-of-materials cost for a design is $110 or less. The design example and associated drivers cost $2500. **Auravision Corp**, Fremont, CA. (510) 252-6800. **Circle No. 336**

PCI-to-Ultra SCSI host adapter cards transfer 40 Mbytes/sec. The Fast!SCSI PCI Ultra products connect directly to the Peripheral Component Interconnect (PCI) bus and will provide double the current 20-Mbyte/sec transfer rate when Ultra SCSI drives become available. The cards let you mix Ultra SCSI and conventional Fast SCSI peripherals on the same SCSI cable. The Fast!SCSI PCI Ultra allows an 8-bit-wide SCSI bus to support 20-Mbyte/sec data-transfer rates and costs $395. The Fast!SCSI PCI Ultra-W provides both fast, 20-Mbyte/sec and wide, 40-Mbyte/sec rates and costs $445. The Fast!SCSI PCI Ultra-W/D accommodates cable lengths up to 25m for differential SCSI products at a 40-Mbyte/sec data-transfer rate. It costs $565. **QLogic Corp**, Costa Mesa, CA. (714) 438-2200. **Circle No. 338**

PCMCIA memory cards offer 40 Mbytes of storage. The PCMCIA Flash Card is available in capacities ranging from 1 to 40 Mbytes. The Type I PCMCIA cards require only 5V for operation and provide 100% disk emulation. A 4-Mbyte version costs $165 (OEM). **M-Systems Inc**, Santa Clara, CA. (408) 654-5820.
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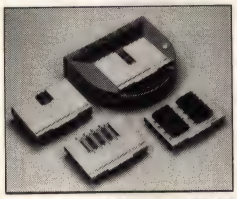

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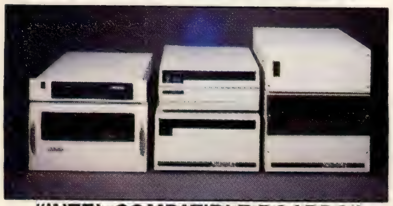

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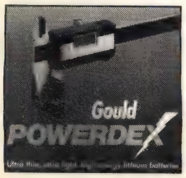

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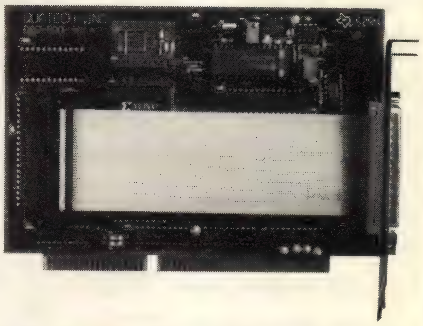

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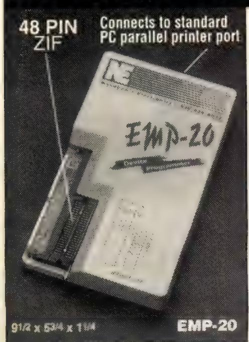

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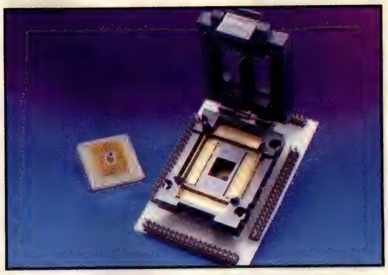

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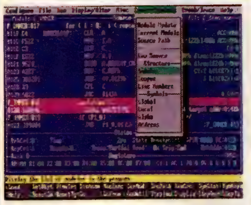

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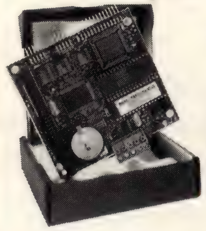

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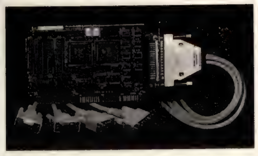

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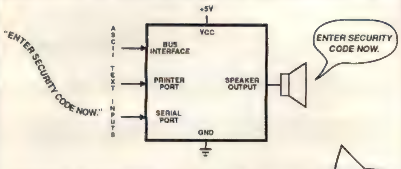

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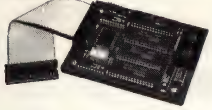

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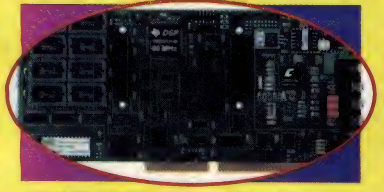

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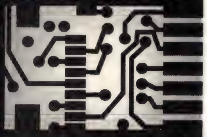

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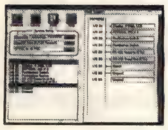

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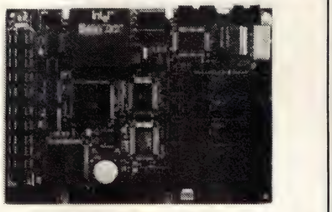

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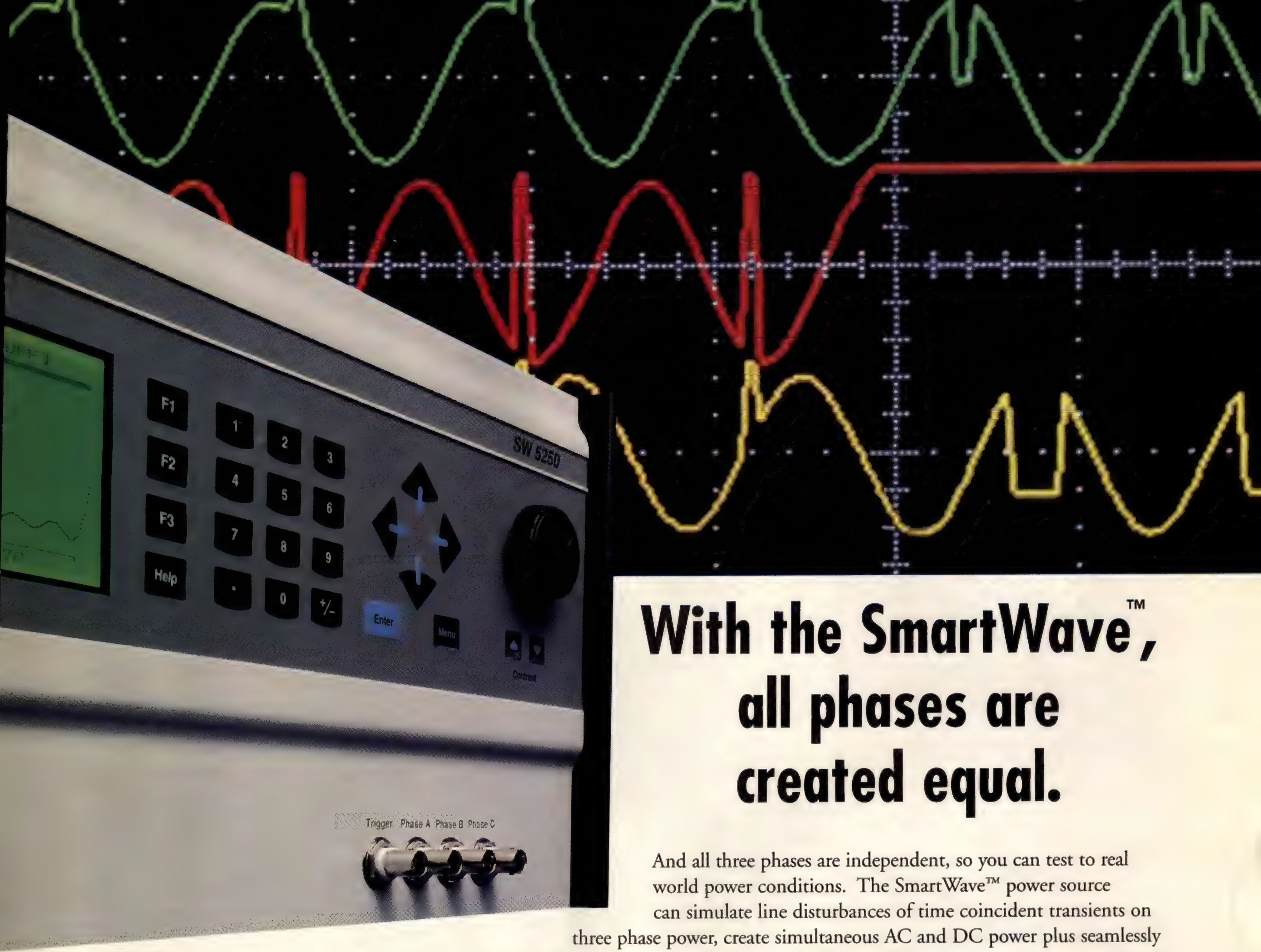

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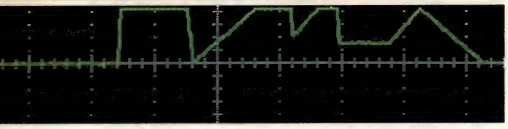

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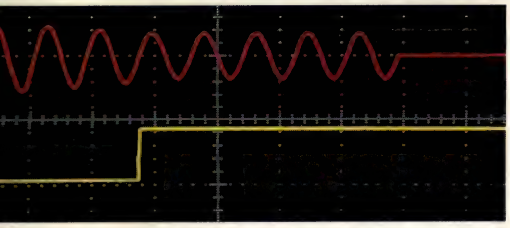

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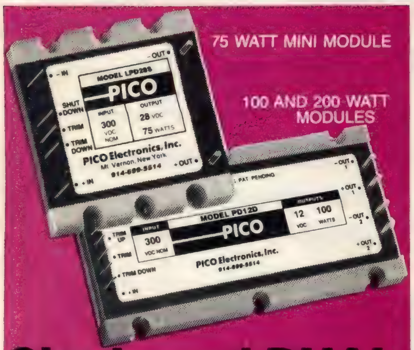

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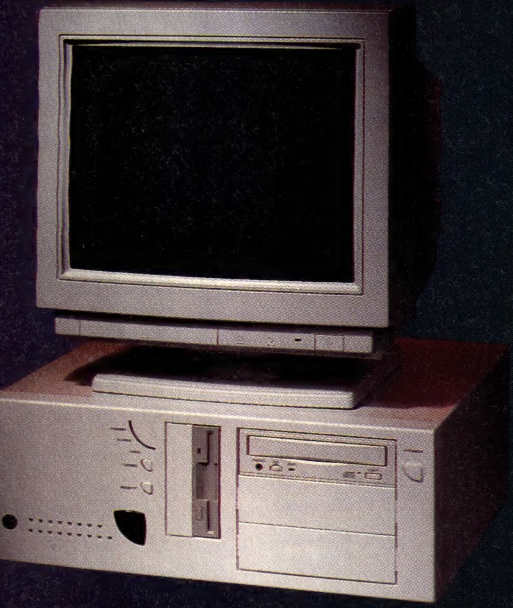

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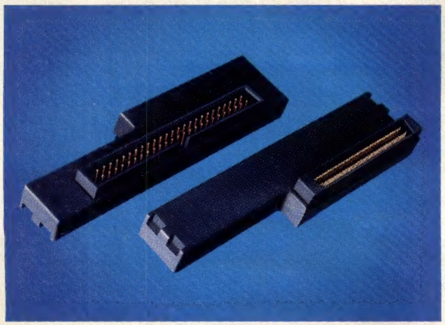

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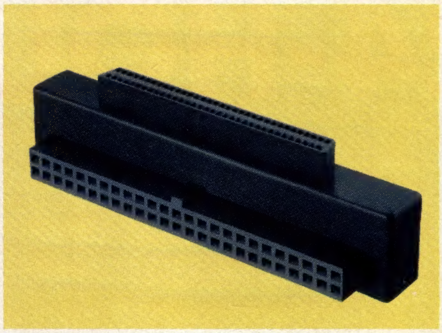

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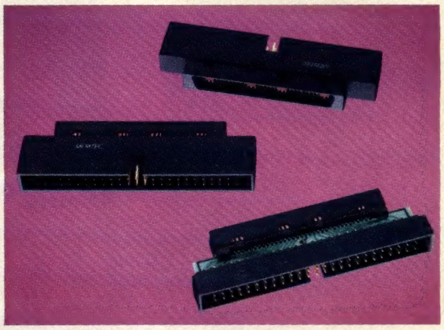
SCSI-3 to SCSI-1 Male-to-Male Adapter is Available For Interfacing Peripherals and Controller Cards.



Meritec's SCSI-3 to SCSI-1 male-to-male adapter allows interfacing between a SCSI-3 peripheral, like a hard disk drive, to a SCSI-1 controller card. The physical package consists of a 68-position .050 x .100 grid SCSI-3 male high density connector to a 50-position .100 x .100 grid SCSI-1 male low density connector. The short overall length between mating faces of the adapter allows for dense packaging. The adapters are available with custom specified pinout and termination. Meritec P/N 940900-4. **CIRCLE NO. 60**

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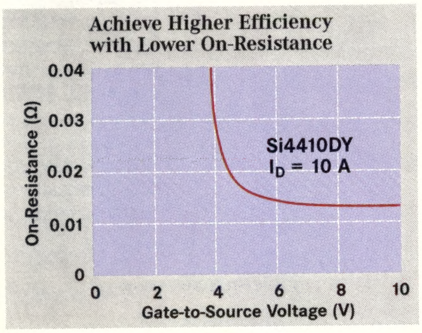

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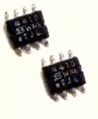

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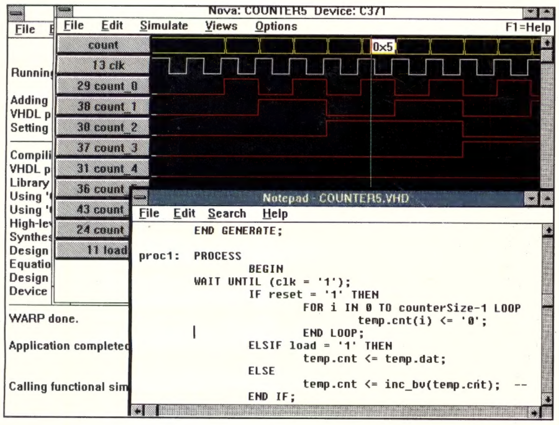
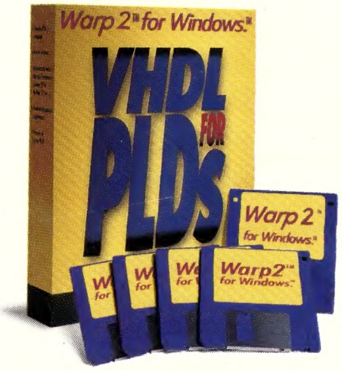


```
Running
Adding
VHDL p
Setting
Compili
VHDL p
Library
Using '
Using '
High-le
Synthes
Design
Equatio
Design
Device
WARP done.
Application complete
Calling functional sim
```

```
        END GENERATE;

proc1:  PROCESS
                BEGIN
        WAIT UNTIL (clk = '1');
                IF reset = '1' THEN
                        FOR i IN 0 TO counterSize-1 LOOP
                                temp.cnt(i) <= '0';
                        END LOOP;
                ELSIF load = '1' THEN
                        temp.cnt <= temp.dat;
                ELSE
                        temp.cnt <= inc_bv(temp.cnt);  --
                END IF;
```



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